

# Cottonwood Schematic Broadwell-ULT

2014-06-09

REV : A00

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*DY : None Installed*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**Cottonwood**

Rev

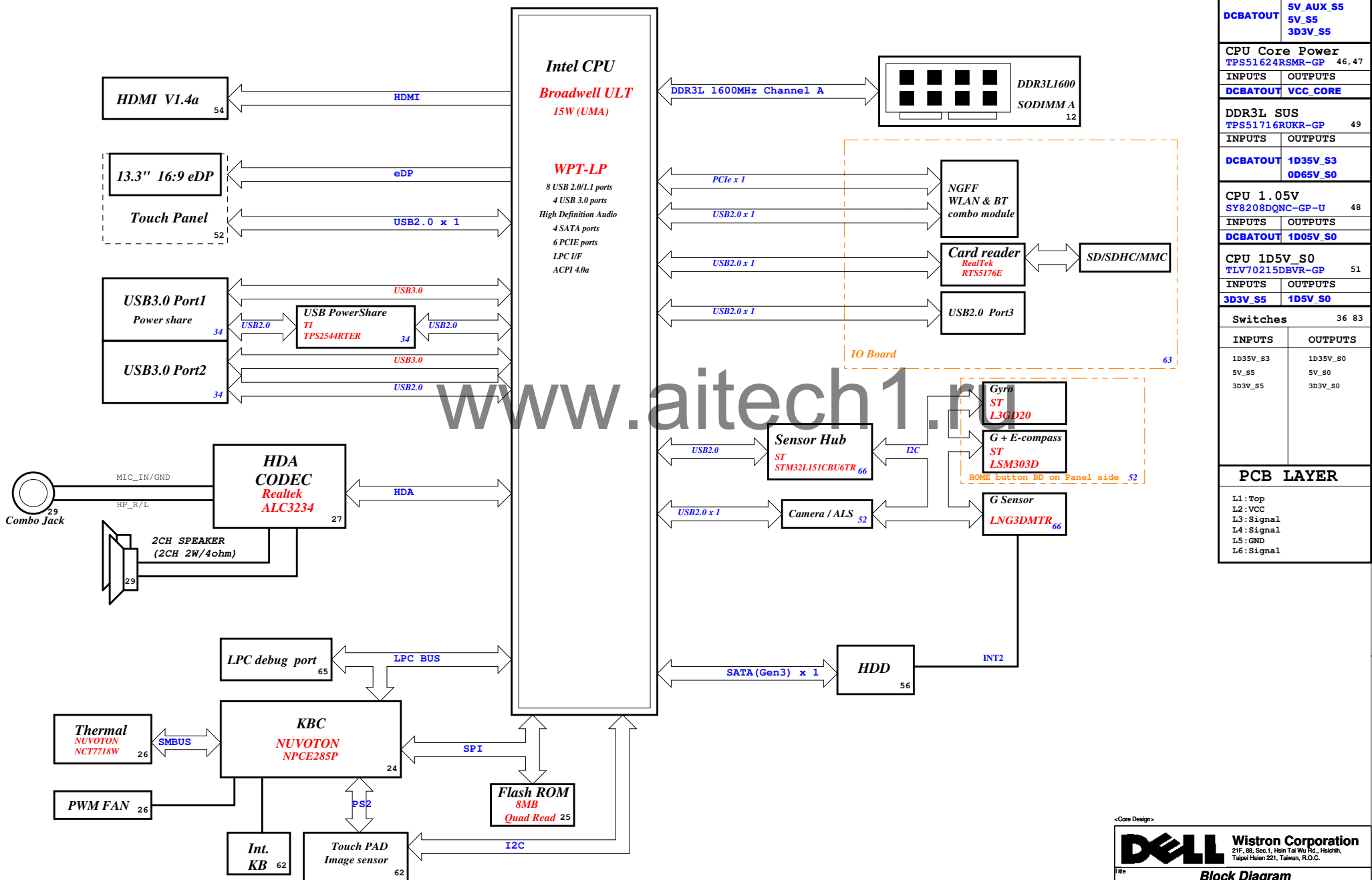
**A00**

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Project code:4PD01V010001  
PCB P/N: 13321  
Revision: A00

# Cottonwood Block Diagram



CHARGER	
BQ24770UYR-GP 44	
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
TPS51624RSMR-GP 46, 47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
SY8208DQNC-GP-U 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
CPU 1D5V_S0	
TLV70215DBVR-GP 51	
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
36 83	
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
PCB LAYER	
L1: Top L2: VCC L3: Signal L4: Signal L5: GND L6: Signal	

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SSID = CPU

**Layout Note:**

Impedance control:50 ohm

[24,44,46] H\_PROCHOT# <<>>

[12] DDR\_PG\_CTRL <<<

**Layout Note:**

Design Guideline:

SM\_RCOMP keep routing length less than 500 mils.

**Layout Note:**

Place close to DIMM

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**CPU (THERMAL/MISC/PM)**

Size  
A4

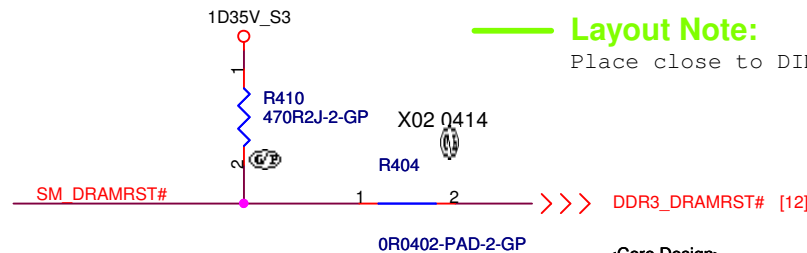
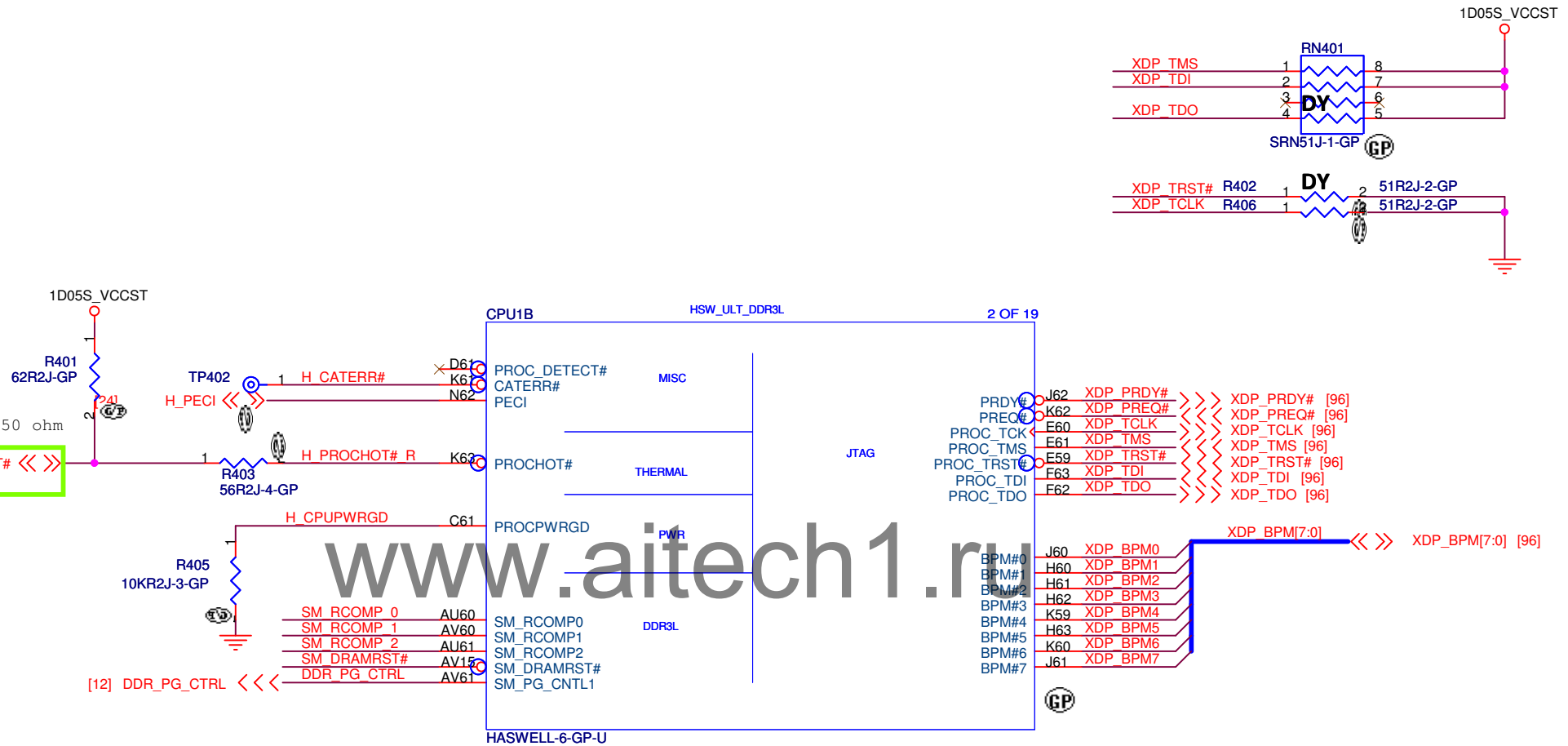
Document Number

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Rev  
**A00**

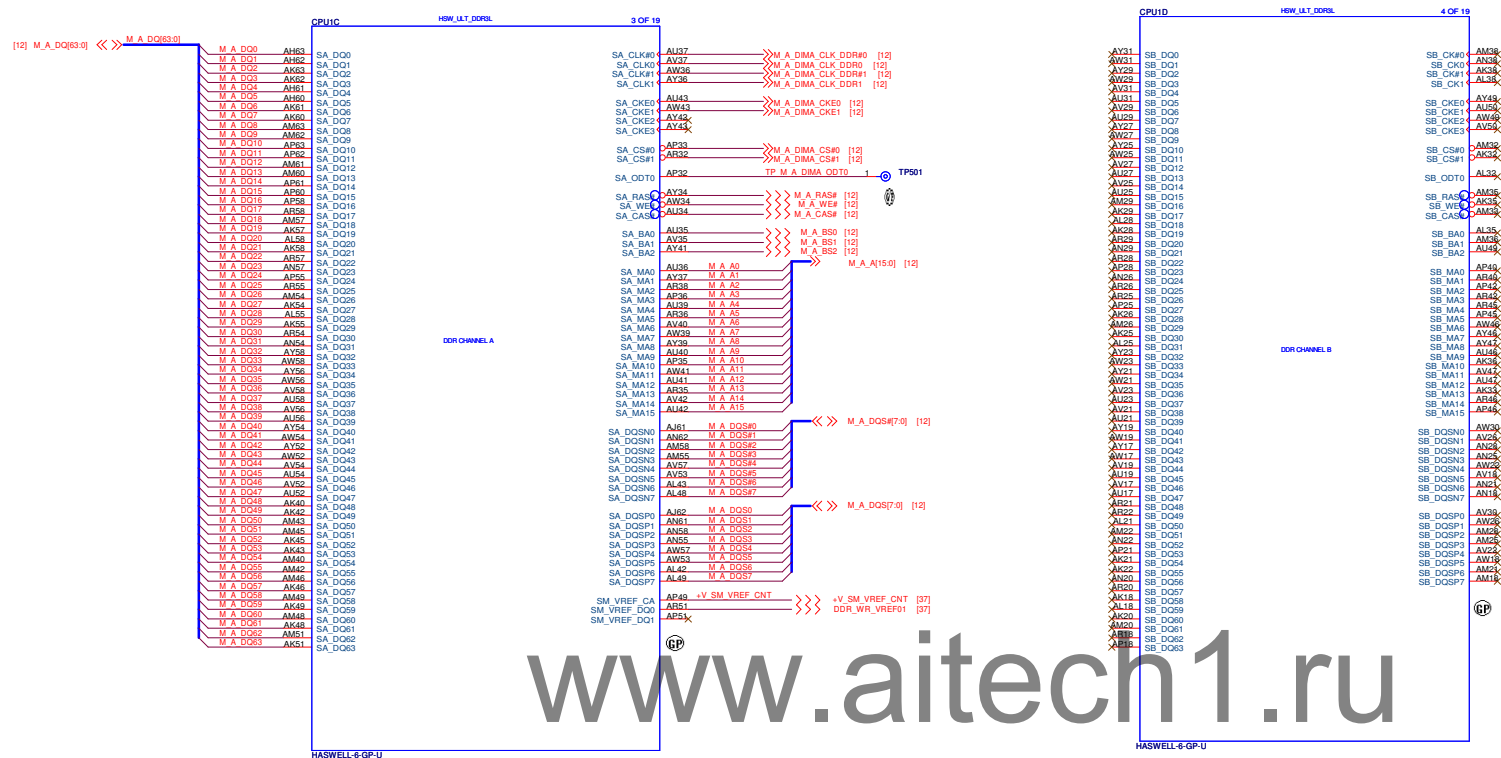
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## DDR3L ball type: Non-Interleaved Type



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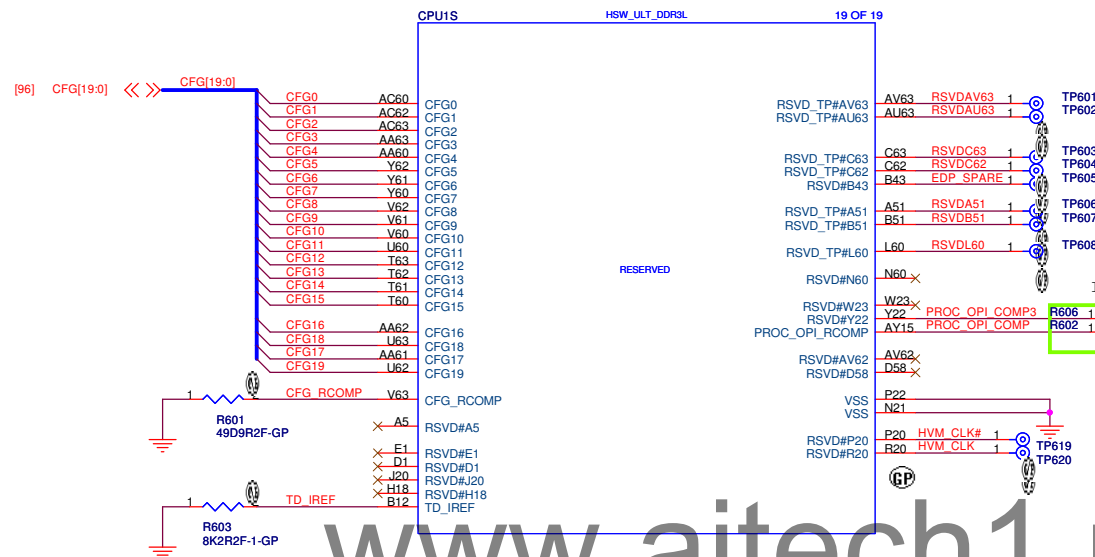
&lt;Core Design&gt;



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CPU (DDR)		
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SSID = CPU



#### 7.4

#### Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD\_TP - these signals should be routed to a test point
- RSVD\_NCTF - these signals are non-critical to function and may be left unconnected

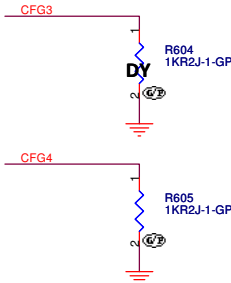
Intel Recommend

#### Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

#514405 PCH strap pin:

Signal Name	Description	Direction / Buffer Type
CFG[19:0]	<b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate Platform Design Guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"><li>• <b>CFG[2:0]:</b> Reserved configuration lane. A test point may be placed on the board for these lanes.</li><li>• <b>CFG[3]: MSR Privacy Bit Feature</b><ul style="list-style-type: none"><li>— 1 = Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting</li><li>— 0 = IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden</li></ul></li><li>• <b>CFG[4]: eDP enable</b><ul style="list-style-type: none"><li>— 1 = Disabled</li><li>— 0 = Enabled</li></ul></li><li>• <b>CFG[19:5]:</b> Reserved configuration lanes. A test point may be placed on the board for these lands.</li></ul>	I/O GTL

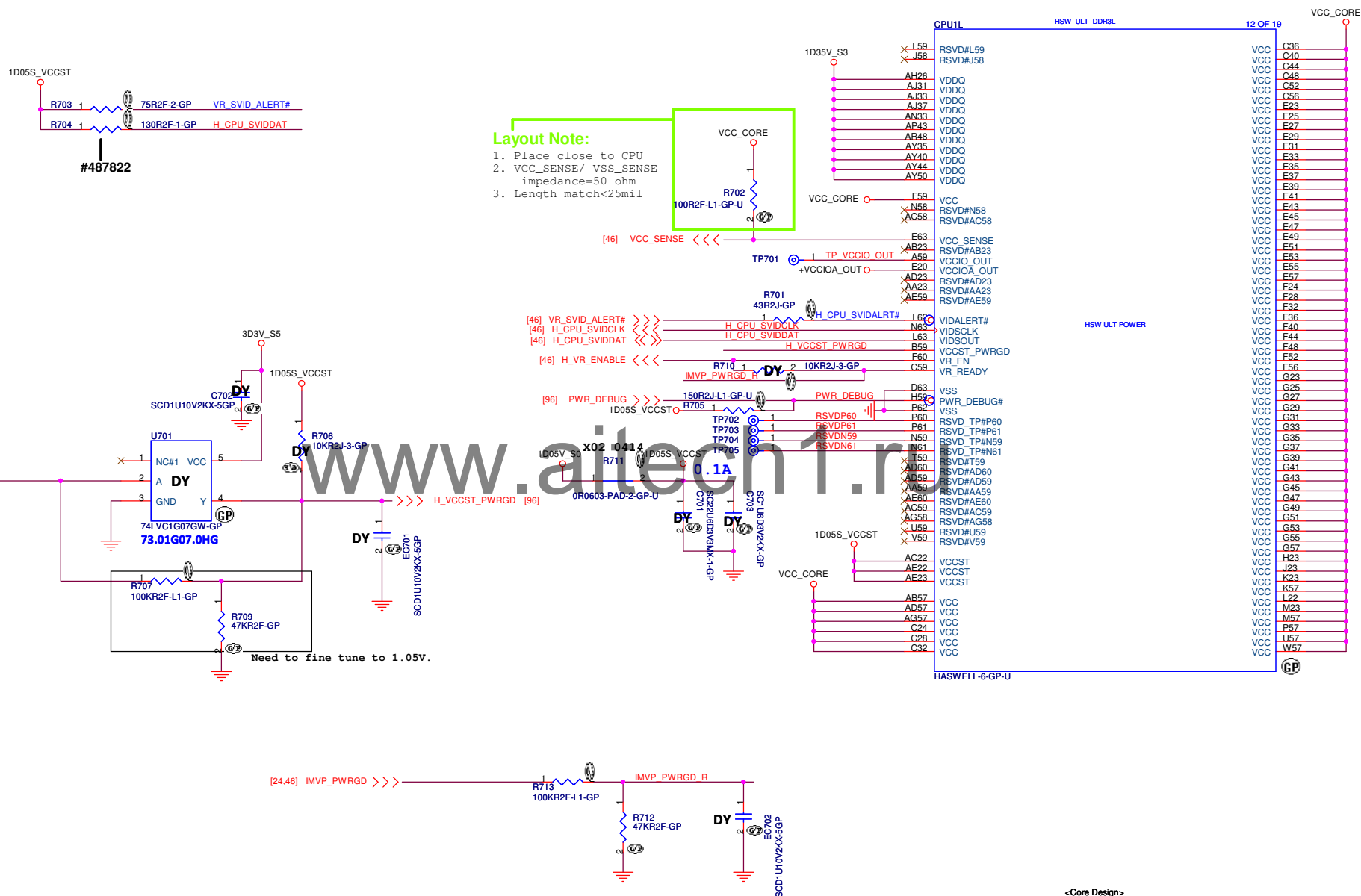


PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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**SSID = CPU**



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Title

**CPU (VCC CORE)**

Size

Document Number

**Cottonwood**

Rev

**A00**

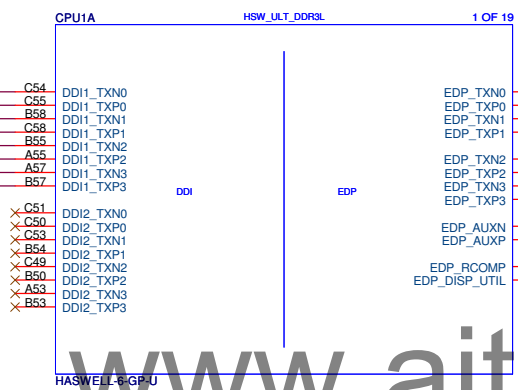
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SSID = CPU

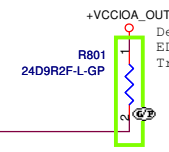
HDMI

[54] HDMI\_DATA2#  
[54] HDMI\_DATA2#  
[54] HDMI\_DATA1#  
[54] HDMI\_DATA1#  
[54] HDMI\_DATA0#  
[54] HDMI\_DATA0#  
[54] HDMI\_CLK#  
[54] HDMI\_CLK#



EDP\_TXN0  
EDP\_TXP0  
EDP\_TXN1  
EDP\_TXP1  
EDP\_TXN2  
EDP\_TXP2  
EDP\_TXN3  
EDP\_TXP3  
EDP\_AUXN  
EDP\_AUXP  
EDP\_RCOMP  
EDP\_DISP\_UTIL

EDP\_TX0\_DN [52]  
EDP\_TX0\_DP [52]  
EDP\_TX1\_DN [52]  
EDP\_TX1\_DP [52]  
EDP\_AUX\_DN [52]  
EDP\_AUX\_DP [52]  
EDP\_COMP  
EDP\_BRIGHTNESS



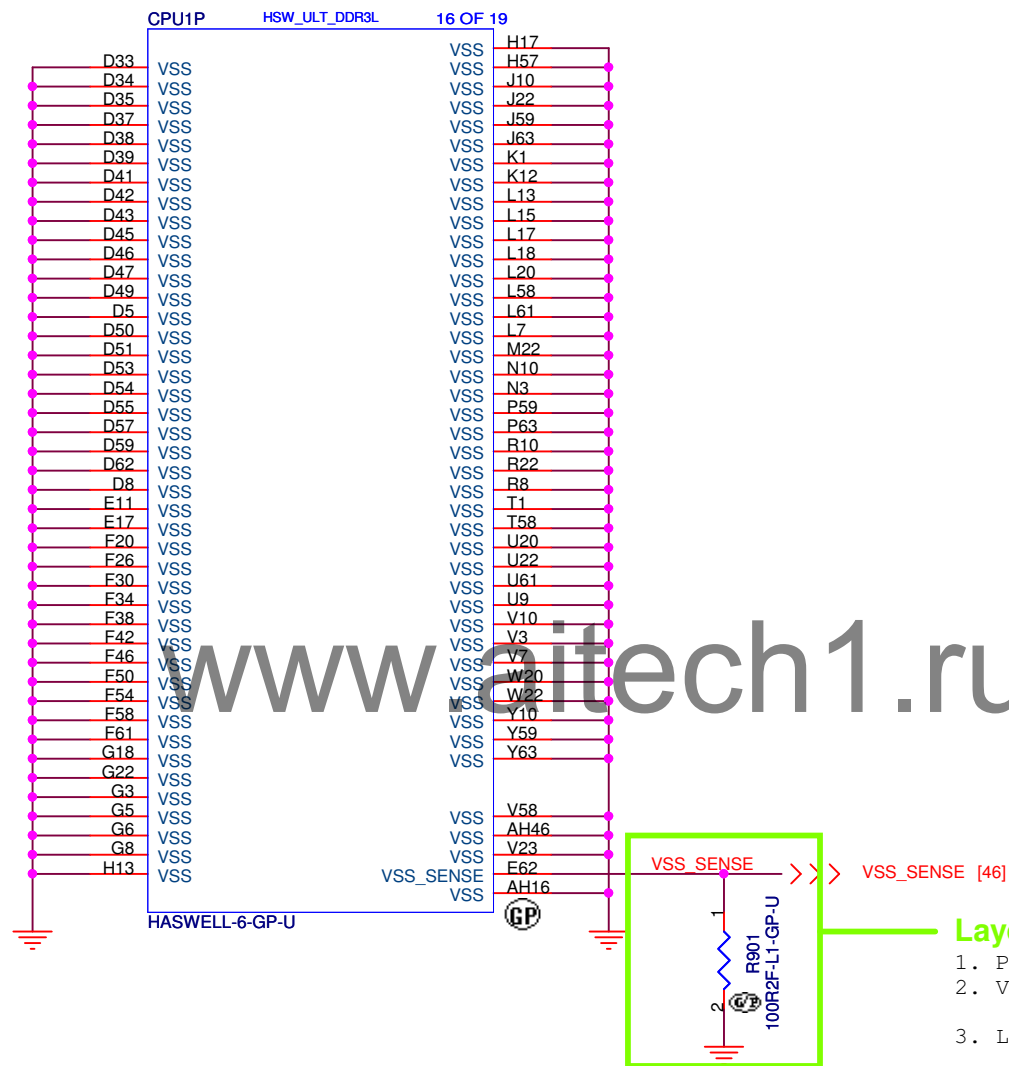
Design Guideline:  
EDP\_COMP keep routing length max 100 mils.  
Trace Width:20 mils.

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Title <b>CPU (DDI/EDP)</b>			
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SSID = CPU



**Layout Note:**

1. Place close to CPU
2. VCC\_SENSE/ VSS\_SENSE impedance=50 ohm
3. Length match<25mil

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**CPU (VSS)**

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A4

Document Number

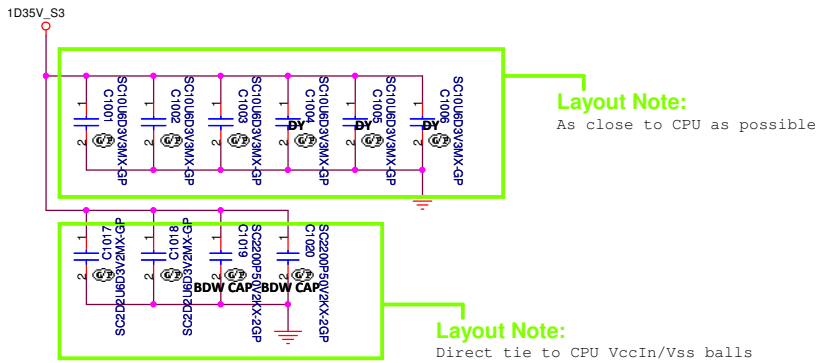
**Cottonwood**

Rev  
**A00**

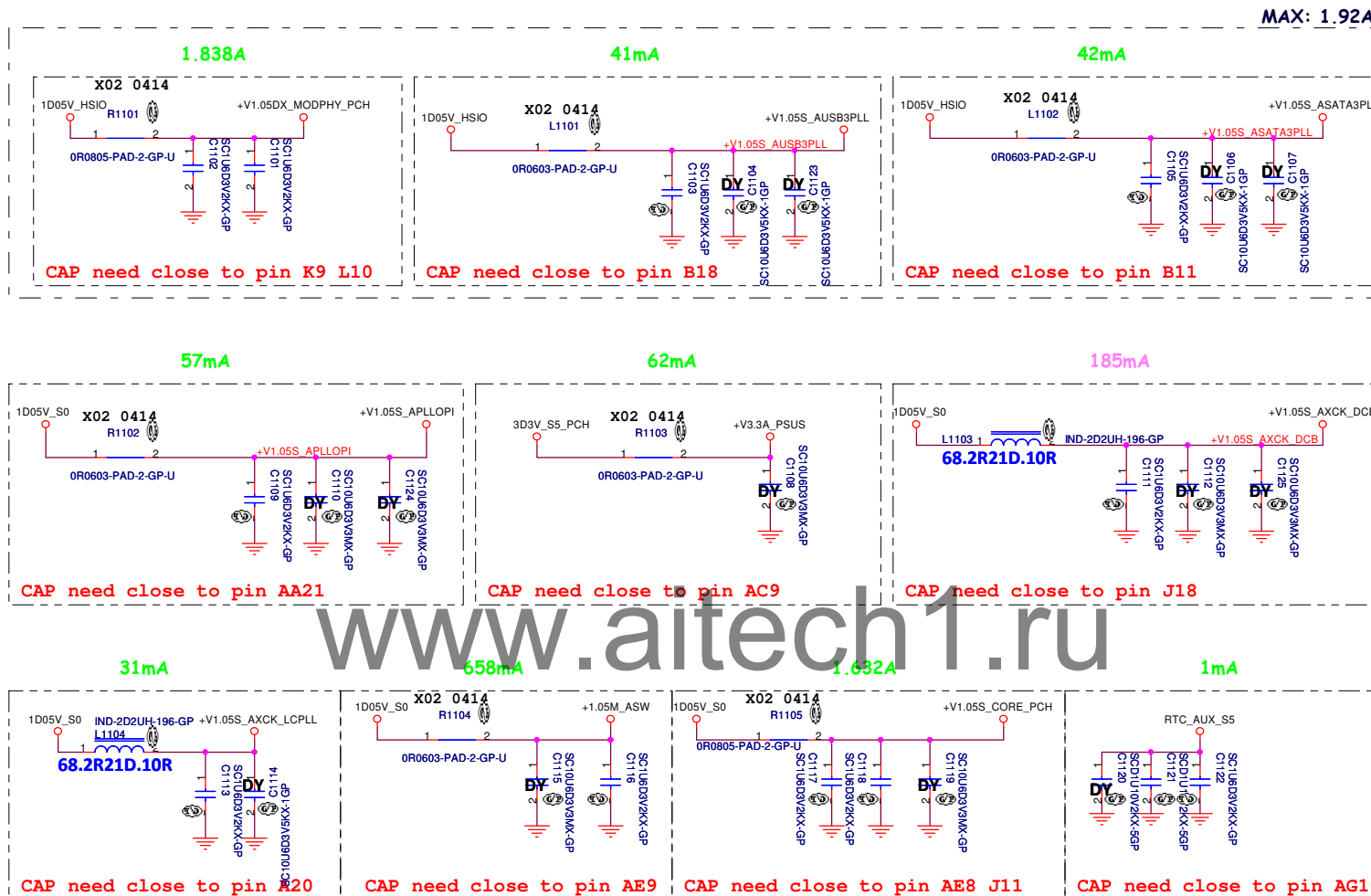
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SSID = CPU



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**CPU (Power CAP2)**

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A3

Document Number

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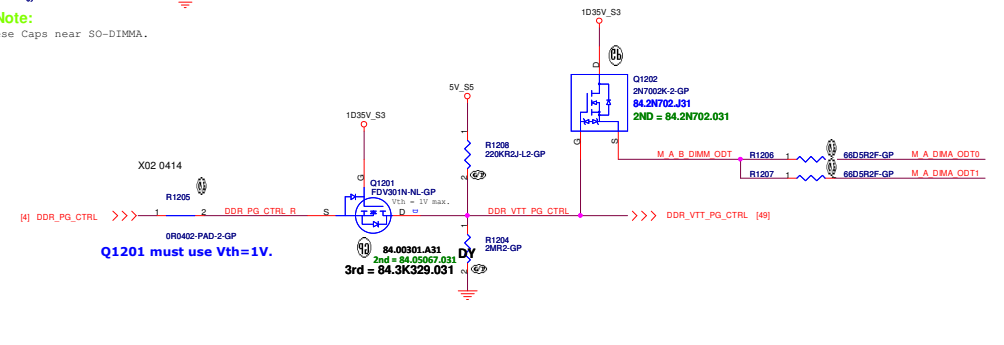
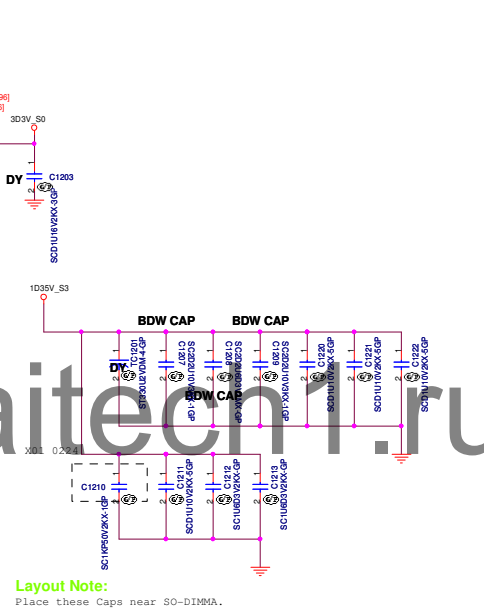
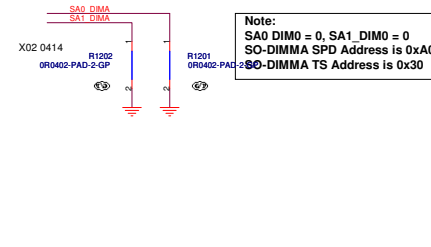
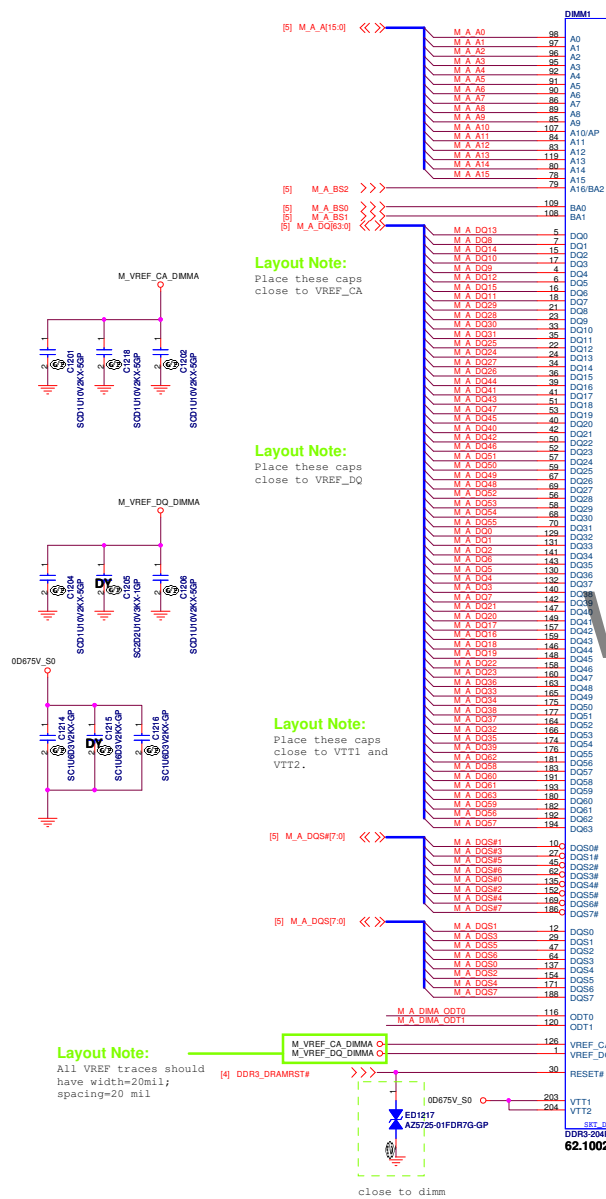
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**SSID = MEMORY**






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(Reserved)DDR3-SODIMM2

Size

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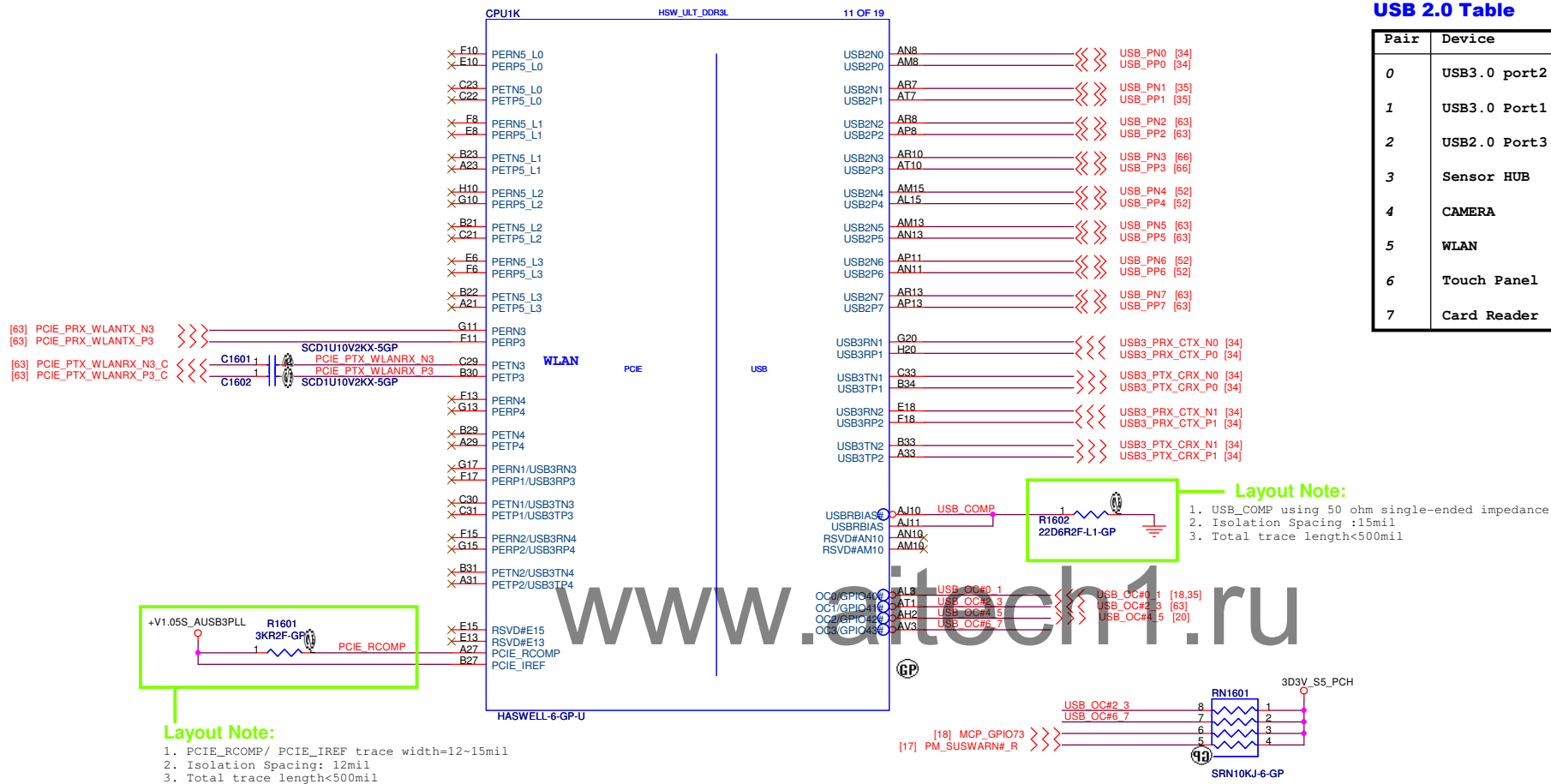
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Title <b>(Reserved)_SODIMM _SODIMM4</b>		
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**SSID = PCH**



## USB 2.0 Table

Pair	Device
0	USB3.0 port2
1	USB3.0 Port1 (Debug Port)
2	USB2.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

- **Layout Note:**

1. USB\_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

**Layout Note:**

1. PCIE\_RCOMP/ PCIE\_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

## PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	N/A	
5 (L0~L3)	N/A	
6 (L3)	HDD	SATA0
6 (L2)	N/A	SATA1
6 (L0~L1)	N/A	

#515621

Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD			GPU	GPU			GPU	GPU	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0

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Title

### **PCH (PCIE/USB)**

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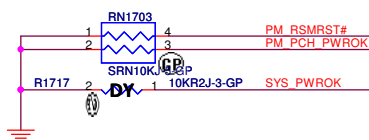
**Cottonwood**

Rev	<b>A00</b>
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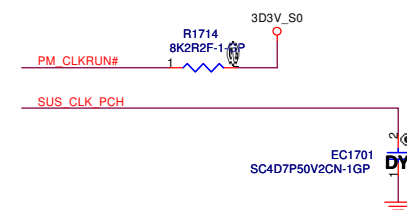
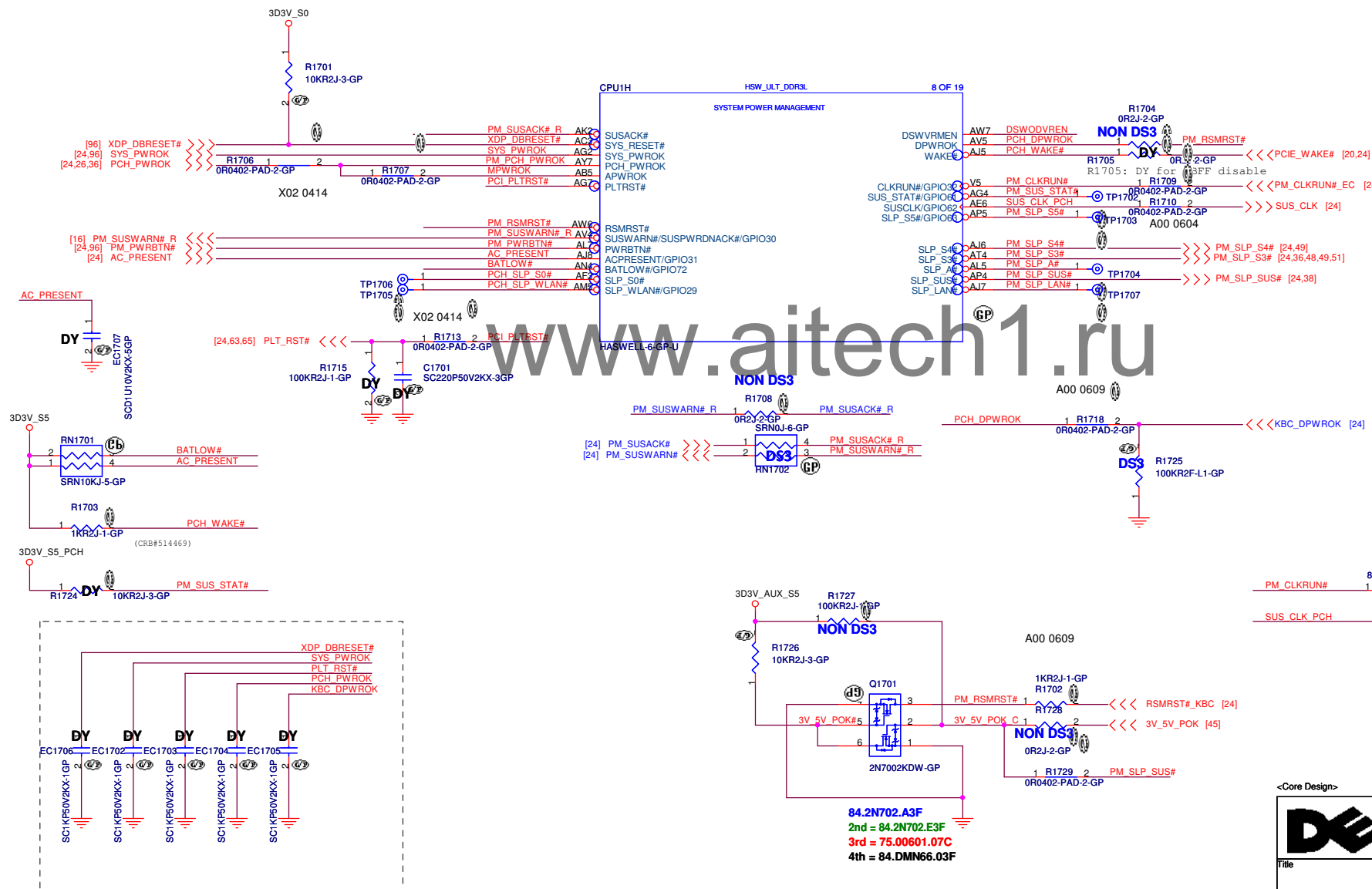
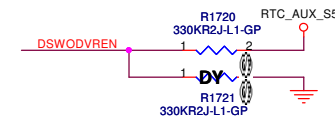
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**SSID = PCH**



**PCH strap pin:**

On Die DSW VR Enable	
DSWODVREN	Low = Disable ★ High = Enable (default)



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DELL

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Title

**PCH (PM)**

Size  
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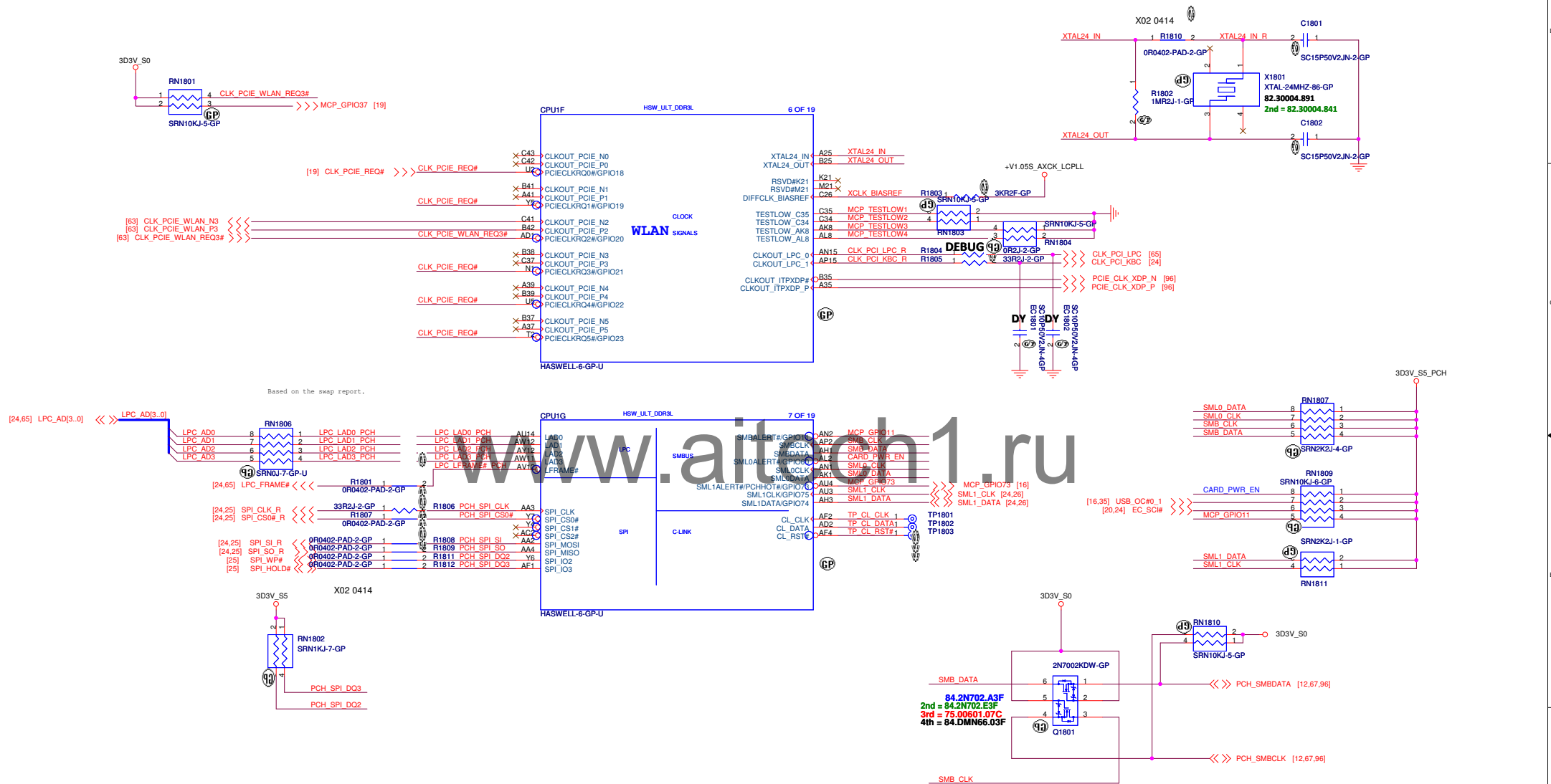
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**SSID = PCH**

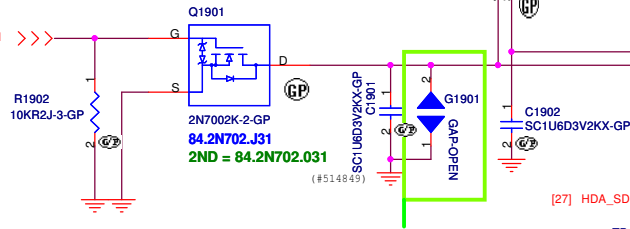
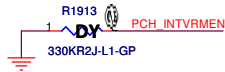


SSID = CPU

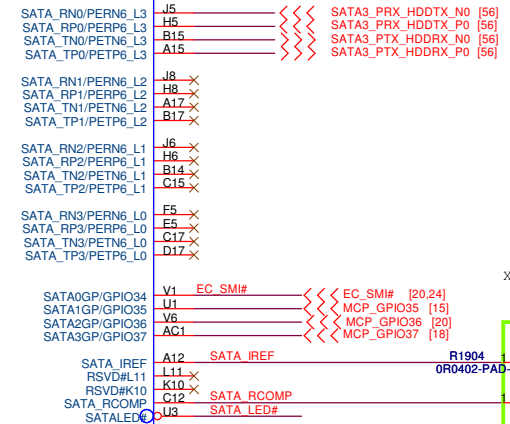
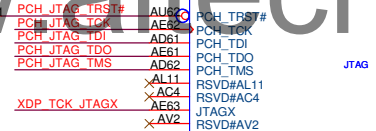
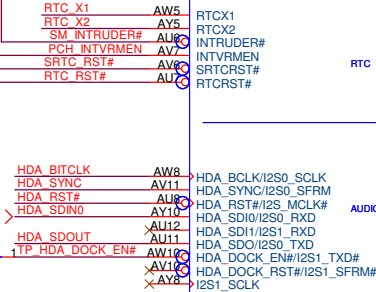
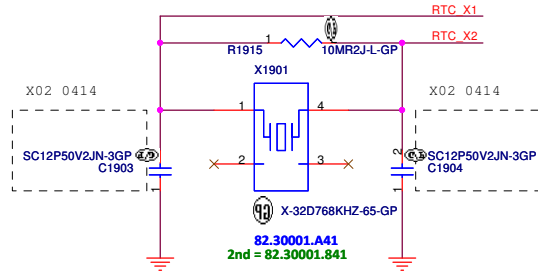
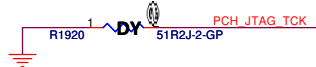
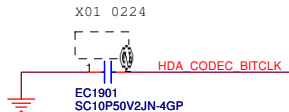
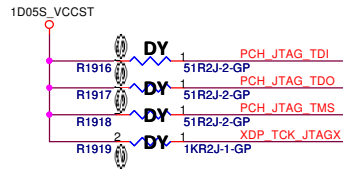
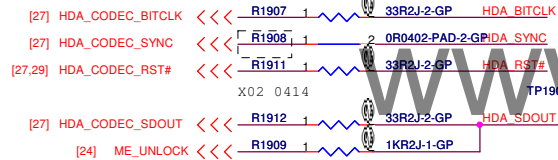
Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

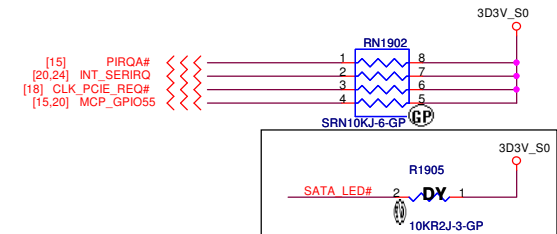
The internal pull-down is disabled after  
PLTRST# deasserts



Layout: Place at the open door area.

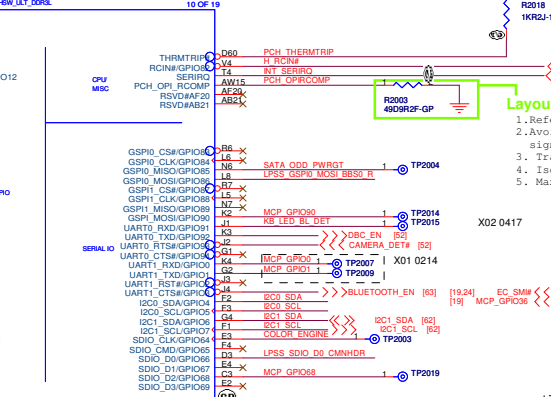
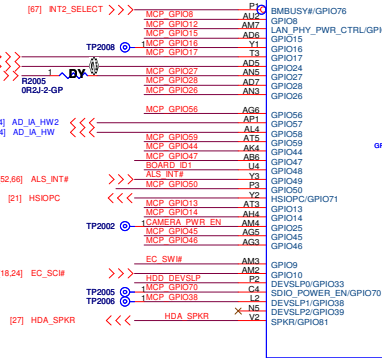
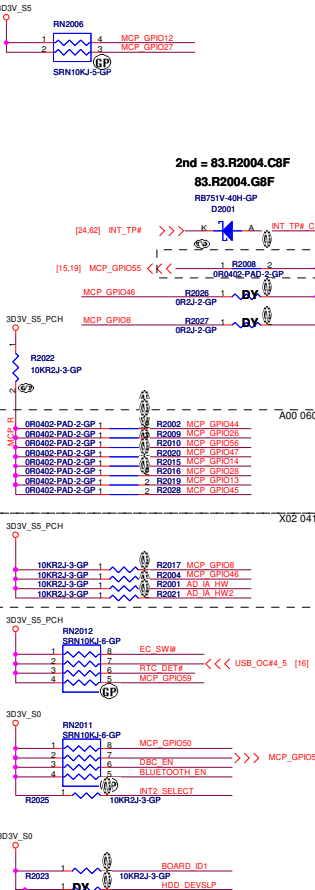


**Layout Note:**  
4mil trace at break-out and 3  
12-15mil trace with <0.2 ohms  
and length total <= 500mils.



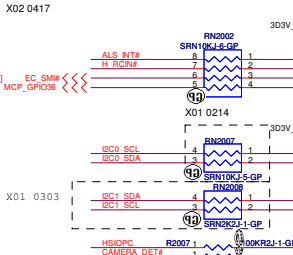
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## SSID = CPU



### Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noise signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



### PCH strap pin

NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after **SLT0EN** is cleared.

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	<p>High = Enable "Top-Block swap" mode (Default)</p> <p>★ Low = Disable "Top-Block swap" mode</p>

The internal pull-down is disabled after BLTDCR# deasserts.

Need SW double confirm if that's needed Top-Block swa

TLS Confidentiality	
GPI015	<p>★ Low = Disable Intel ME Crypto TLS</p> <p>High = Enable Intel ME Crypto TLS</p>

The internal pull-down is disabled after  
BSMRST# deasserts.

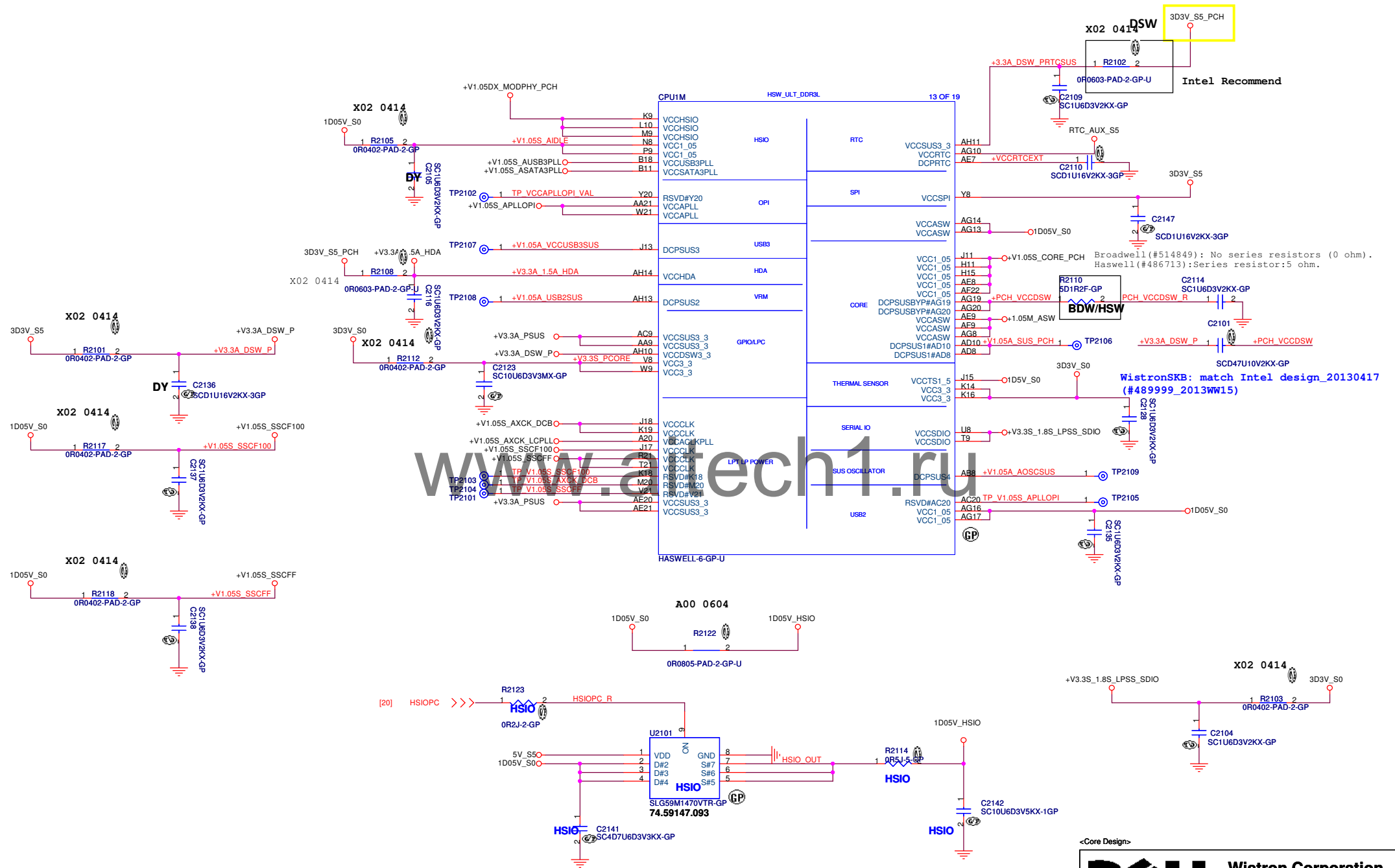
Boot BIOS Strap Bit BBS	
Boot BIOS Destination	★ Low = SPI High = LPC

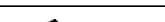
The internal pull-down is disabled after  
PI TRST# deasserts

Need double confirm. GPIO table set to GPI if that's needed PH or PL

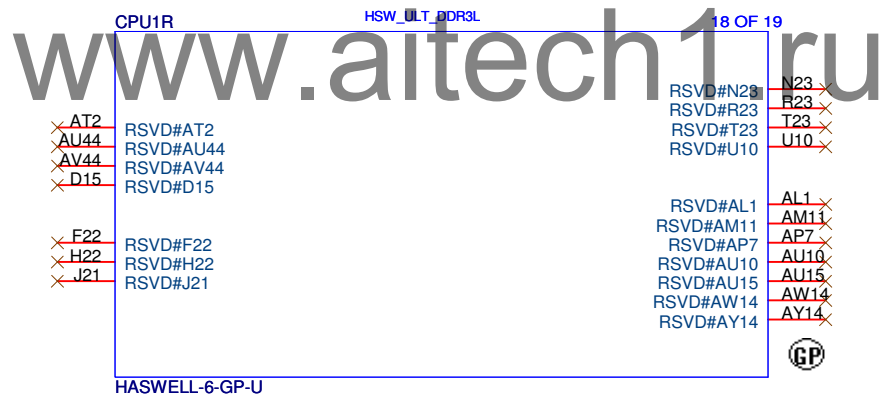
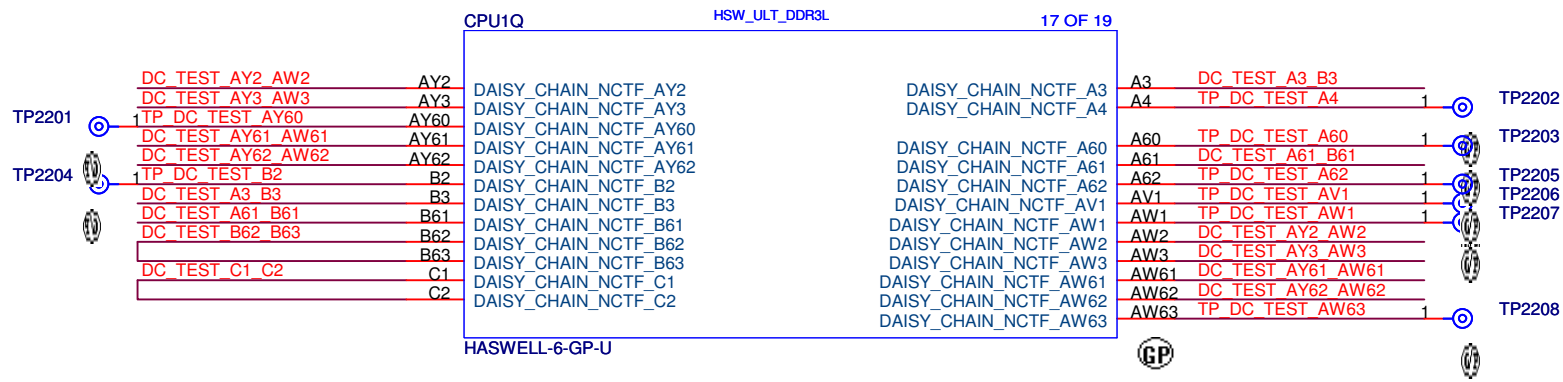


**SSID = CPU**




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Title			
<p><b><i>CPU (POWER2)</i></b></p> <p><b><i>Cottonwood</i></b></p>			
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SSID = PCH



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Title

CPU (RSVD)

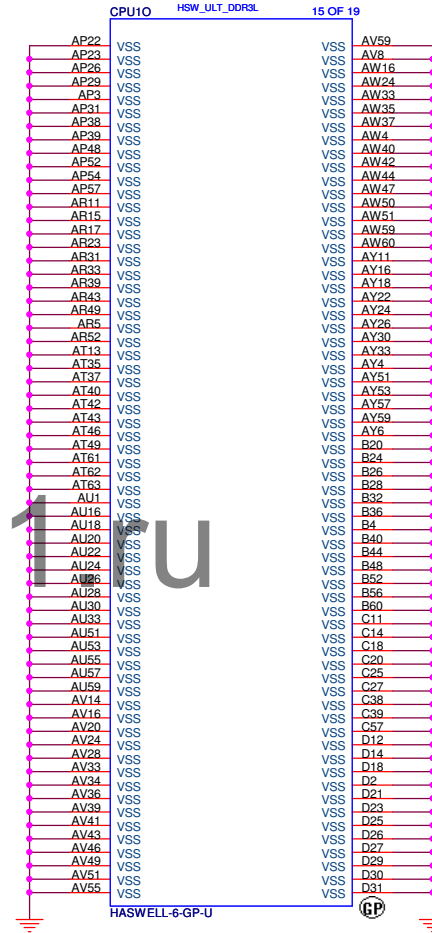
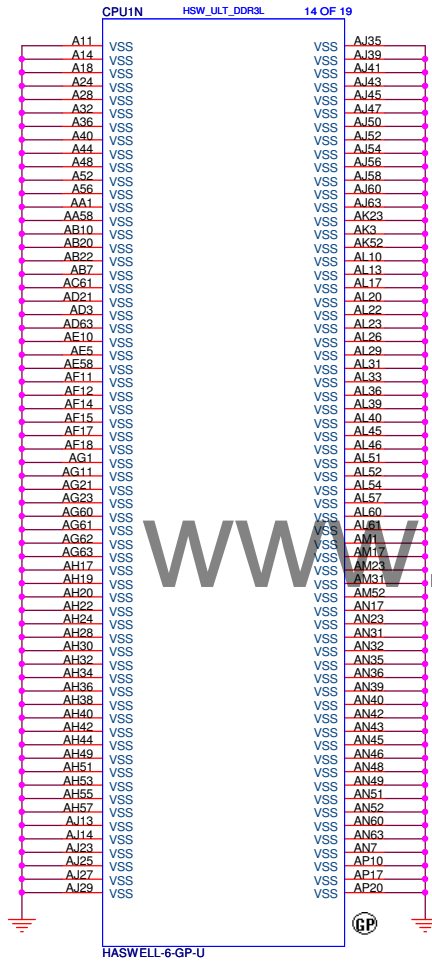
SizeA4

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RevA00

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SSID = PCH



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Title

**CPU(VSS)**

Size  
A3

Document Number

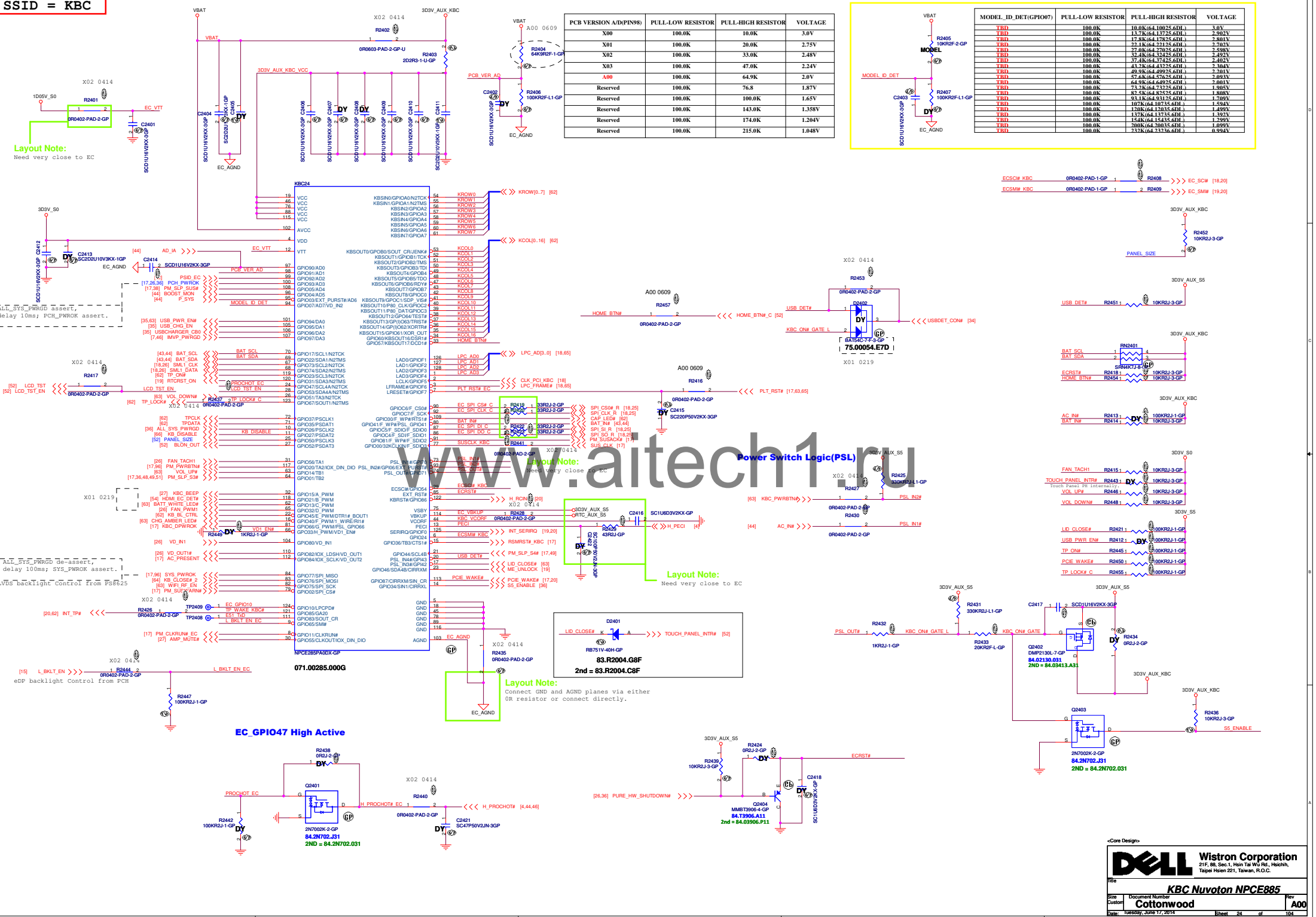
**Cottonwood**

Rev  
**A00**

Date: Tuesday, June 17, 2014

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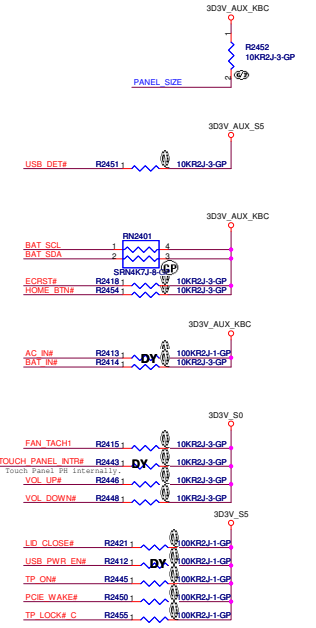
SSID = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

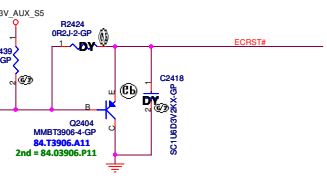
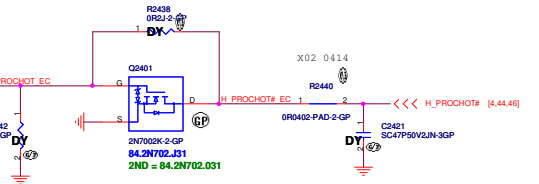
MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1B0	100.0K	10.0K(64.10025.GD1)	3.0V
1B0	100.0K	13.2K(64.11735.GD1)	2.900V
1B0	100.0K	17.8K(64.17825.GD1)	2.801V
1B0	100.0K	22.1K(64.23135.GD1)	2.702V
1B0	100.0K	27.0K(64.27025.GD1)	2.598V
1B0	100.0K	32.4K(64.32425.GD1)	2.492V
1B0	100.0K	37.4K(64.37435.GD1)	2.393V
1B0	100.0K	43.2K(64.43235.GD1)	2.301V
1B0	100.0K	49.0K(64.49025.GD1)	2.200V
1B0	100.0K	57.6K(64.57625.GD1)	2.093V
1B0	100.0K	64.0K(64.64025.GD1)	2.000V
1B0	100.0K	73.2K(64.73235.GD1)	1.905V
1B0	100.0K	82.5K(64.82525.GD1)	1.800V
1B0	100.0K	93.1K(64.93135.GD1)	1.700V
1B0	100.0K	107.0K(64.10735.GD1)	1.594V
1B0	100.0K	120.0K(64.12035.GD1)	1.490V
1B0	100.0K	137.0K(64.13735.GD1)	1.392V
1B0	100.0K	154.0K(64.15435.GD1)	1.290V
1B0	100.0K	200.0K(64.20035.GD1)	1.090V
1B0	100.0K	232.0K(64.23235.GD1)	0.994V

ECSCW# KBC 0R0402-PAD-1-GP 1 R2408 >>> EC\_SCW# [18.20]  
ECSCW# KBC 0R0402-PAD-1-GP 1 R2409 >>> EC\_SMW# [19.20]



Layout Note:  
Connect GND and AGND planes via either  
0R resistor or connect directly.

EC\_GPIO47 High Active



<Core Design>

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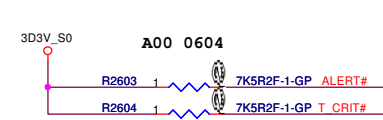
File  
Size  
Custom  
Date

Document Number  
**KBC Nuvoton NPCE885**  
**Cottonwood**  
Tuesday, June 17, 2014

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**A00**  
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**SSID = Thermal**

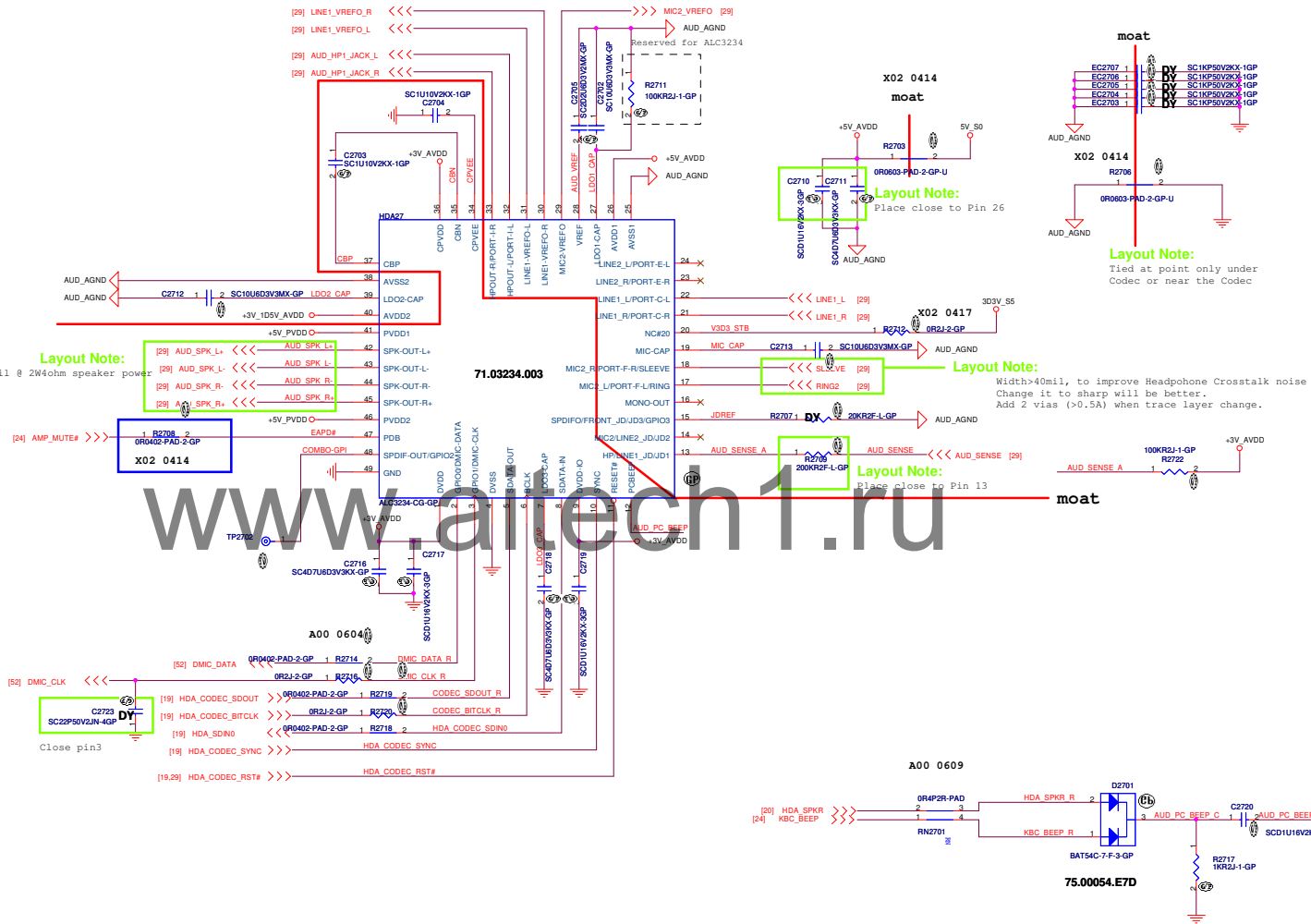
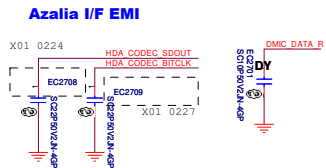
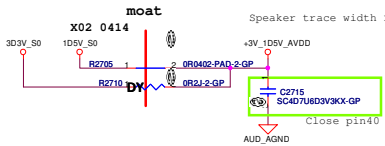
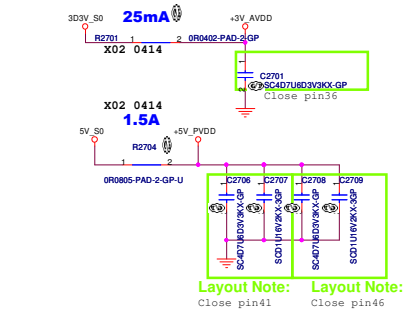


2N7002K-2-GP  
84.2N702.J31  
2ND = 84.2N702.031  
3rd = 84.07002.J31  
4th = 84.2N702.W31

3D3V\_S0



SSID = AUDIO



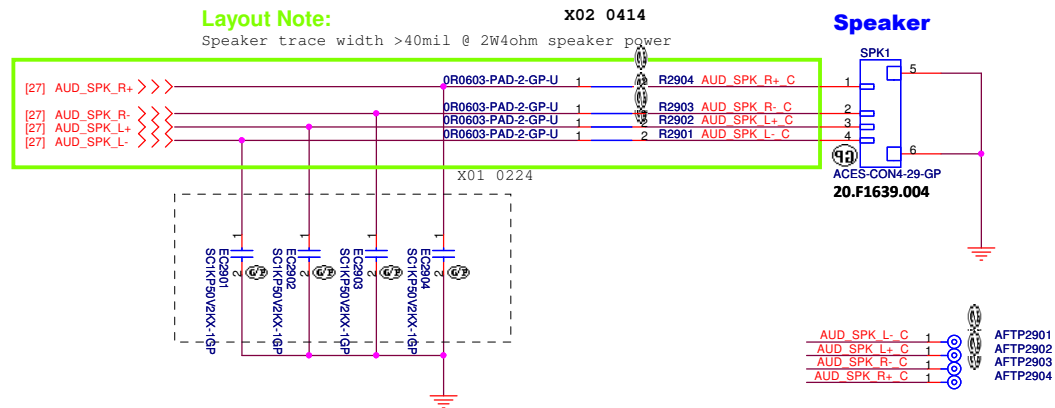
SSID = AUDIO

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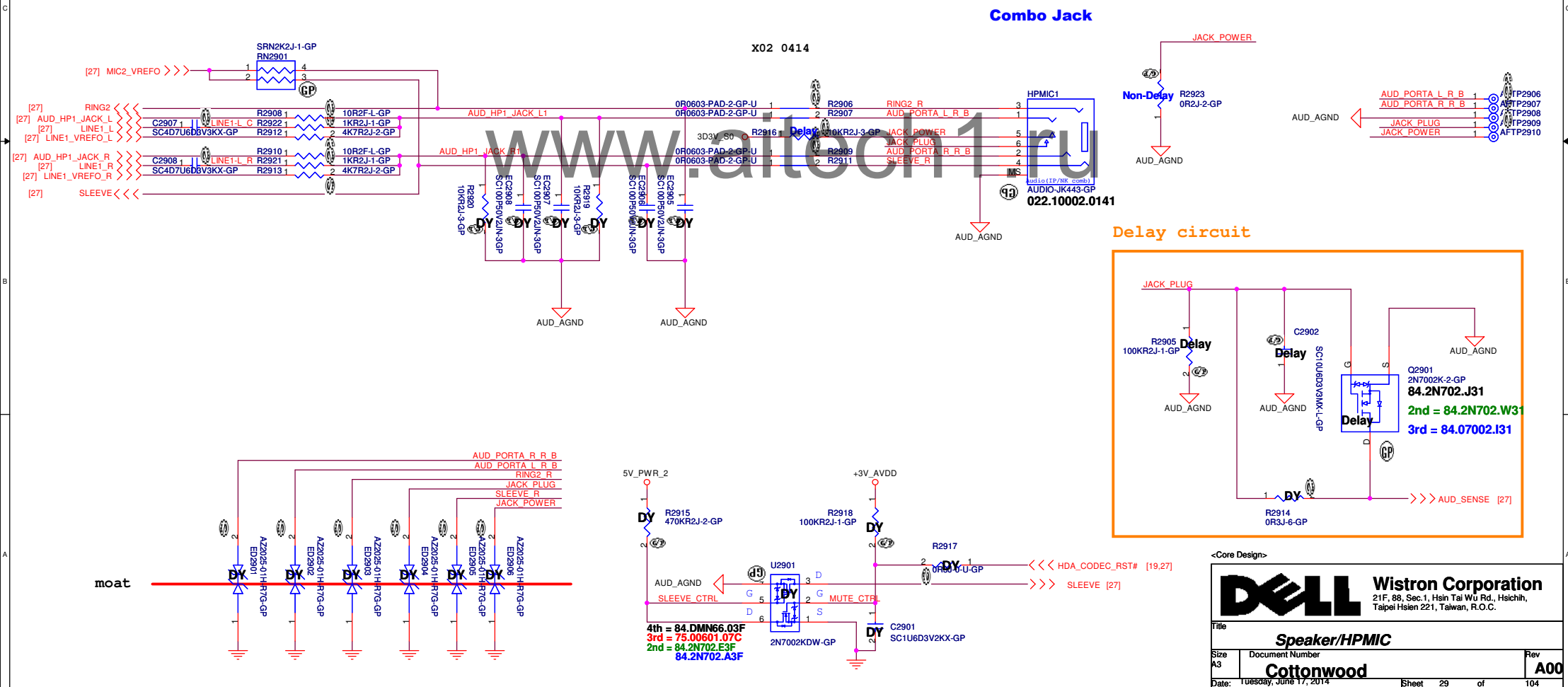
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SSID = AUDIO



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



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SSID = LOM

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Title

**XFOM&RJ45**

Size  
A3

Document Number

**Cottonwood**

Rev

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Date: Tuesday, June 17, 2014

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(Blanking)  
www.aitech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)Card Reader</b>			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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(Blanking)

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**(Reserved)**

Size  
A3

Document Number

**Cottonwood**

Rev

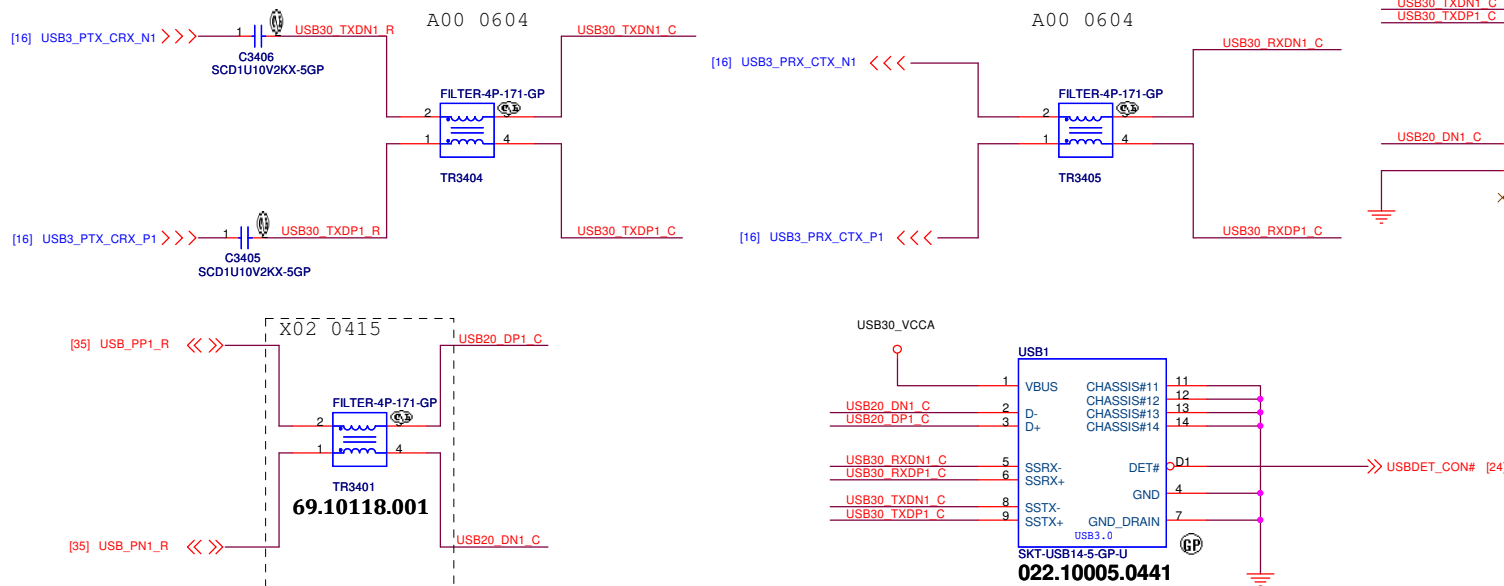
**A00**

Date: Tuesday, June 17, 2014

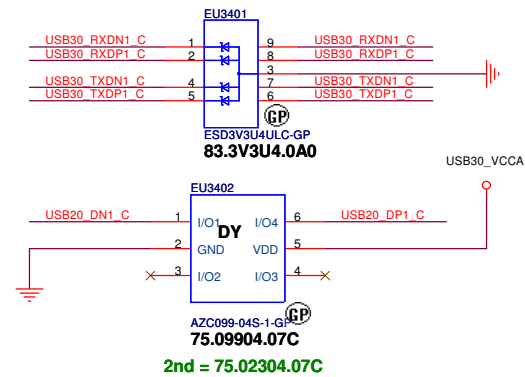
Sheet 33 of 104

SSID = USB

## USB3.0 Port1



X02 0416

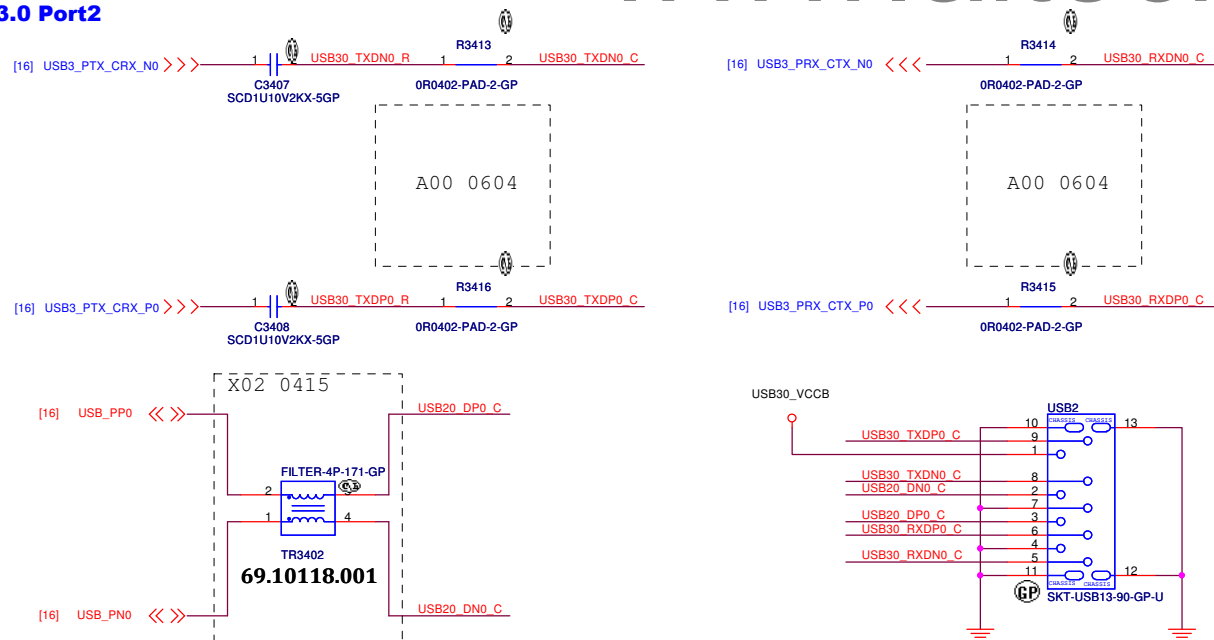


### USB 3.0 Connector Pin definition

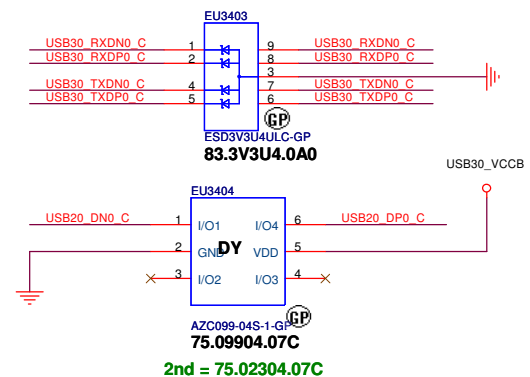
Pin	Definition
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

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## USB3.0 Port2



X02 0416



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Title		
USB 3.0		
Size	Document Number	Rev
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[illegible]

Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
<b>CDP</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>
<b>DCP Auto</b>	<b>0</b>	<b>1</b>	<b>1</b>	<b>X</b>

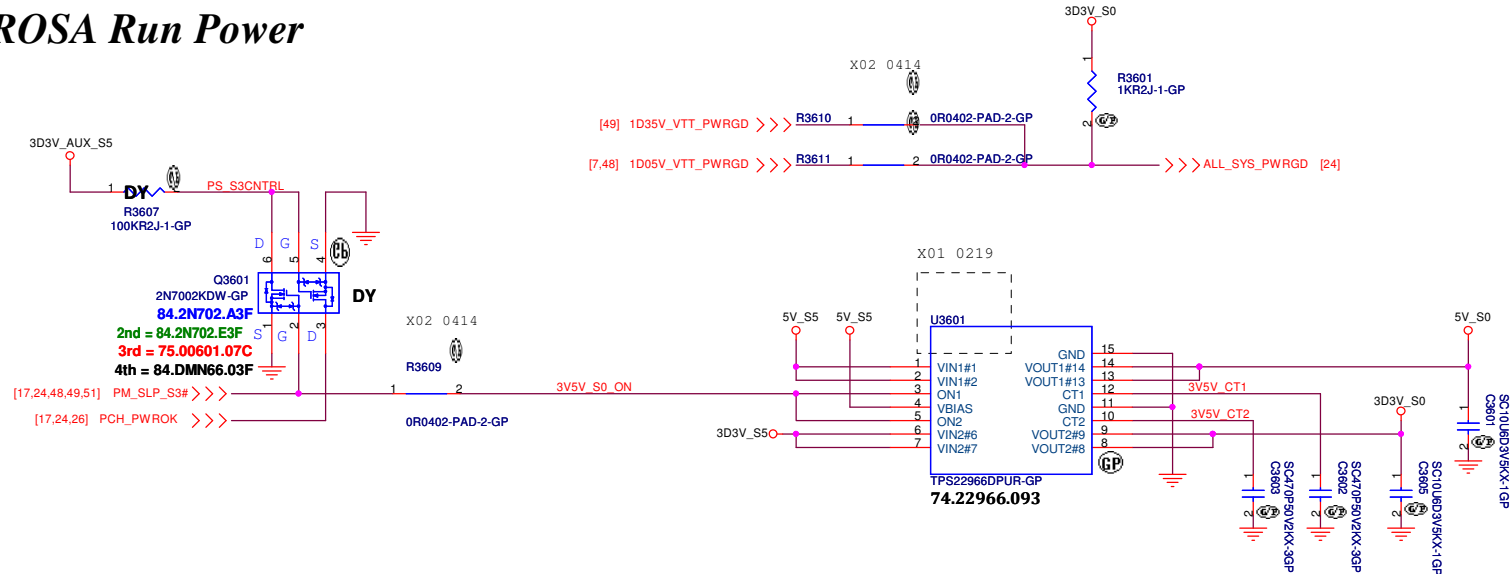
[illegible]

78.10710.52L

SSID = Reset.Suspend

Power Good

ROSA Run Power



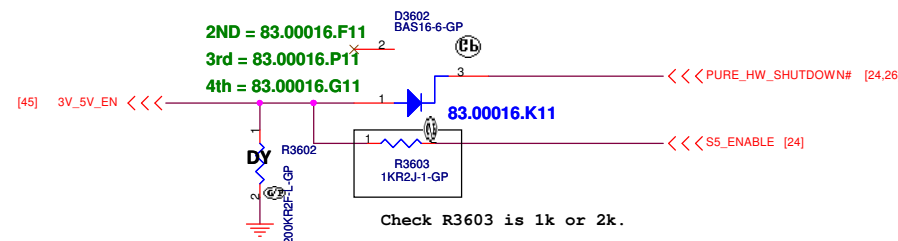
5V\_S0

5V\_S0 Consumption  
Peak current 5A

3D3V\_S0

3D3V\_S0 Consumption  
Peak current 2.5A

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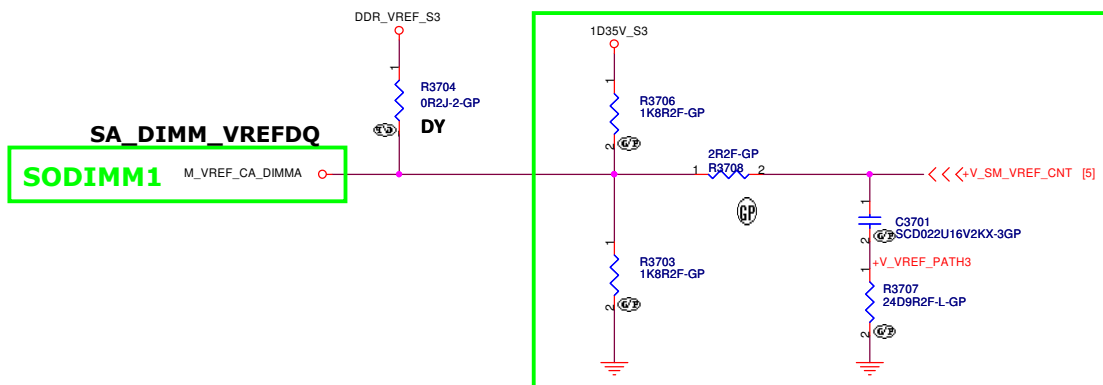
<Core Design>



SSID = Reset.Suspend

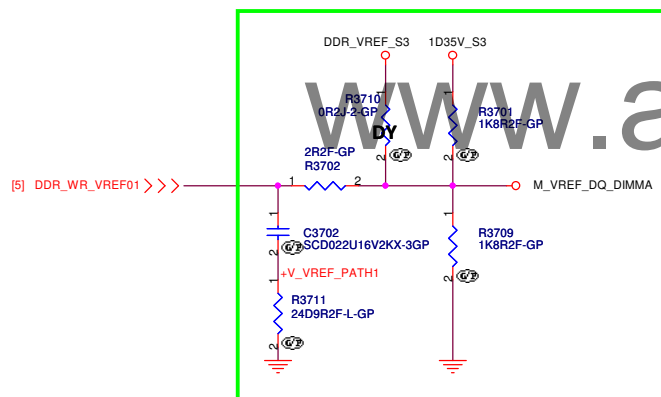
Layout Note:

Place Close SO-DIMM1



Layout Note:

Place Close SO-DIMM1



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Title

**S3 Reduction Circuit**

Size  
A3

Document Number

**Cottonwood**

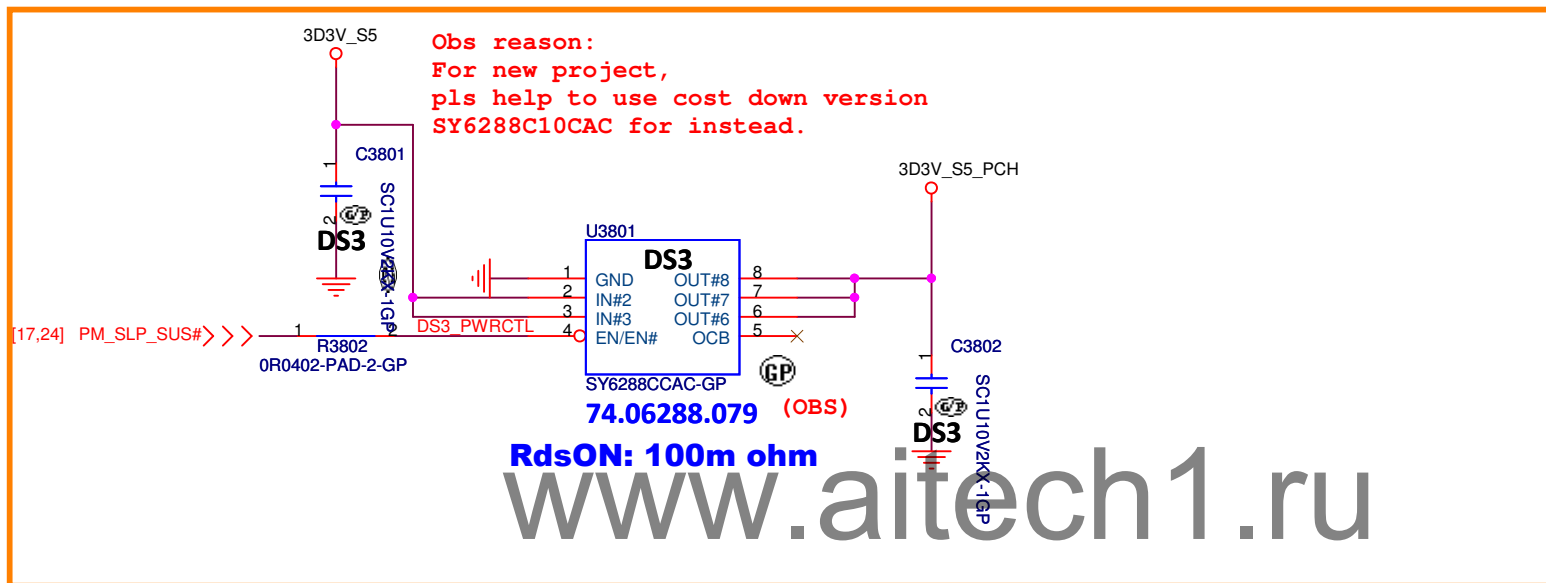
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A00



Obs reason:  
For new project,  
pls help to use cost down version  
SY6288C10CAC for instead.



DS3

<Core Design>



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Title

**DSW**

Size  
A4

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Title  
**(Reserved) 1D05\_M**

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(Blanking)

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<Core Design>

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Title		
<b><i>Reserved</i></b>		
Size A4	Document Number <b><i>Cottonwood</i></b>	Rev <b><i>A00</i></b>
Date: Tuesday, June 17, 2014		Sheet 40 of 104

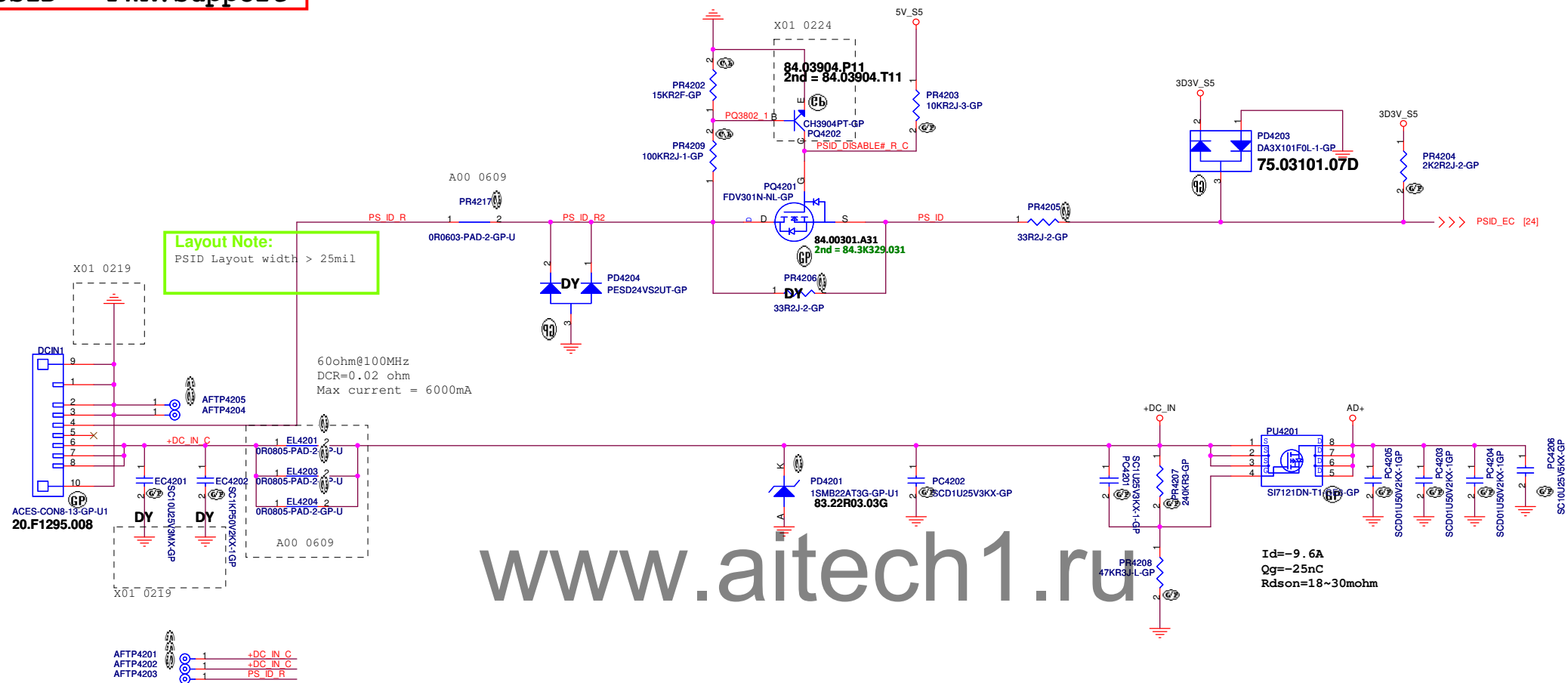
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Title			
<i>Reserved</i>			
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```
SSID = PWR.Support
```



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## <Core Design>



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Title

***DCIN***

Size  
A3

Document Number
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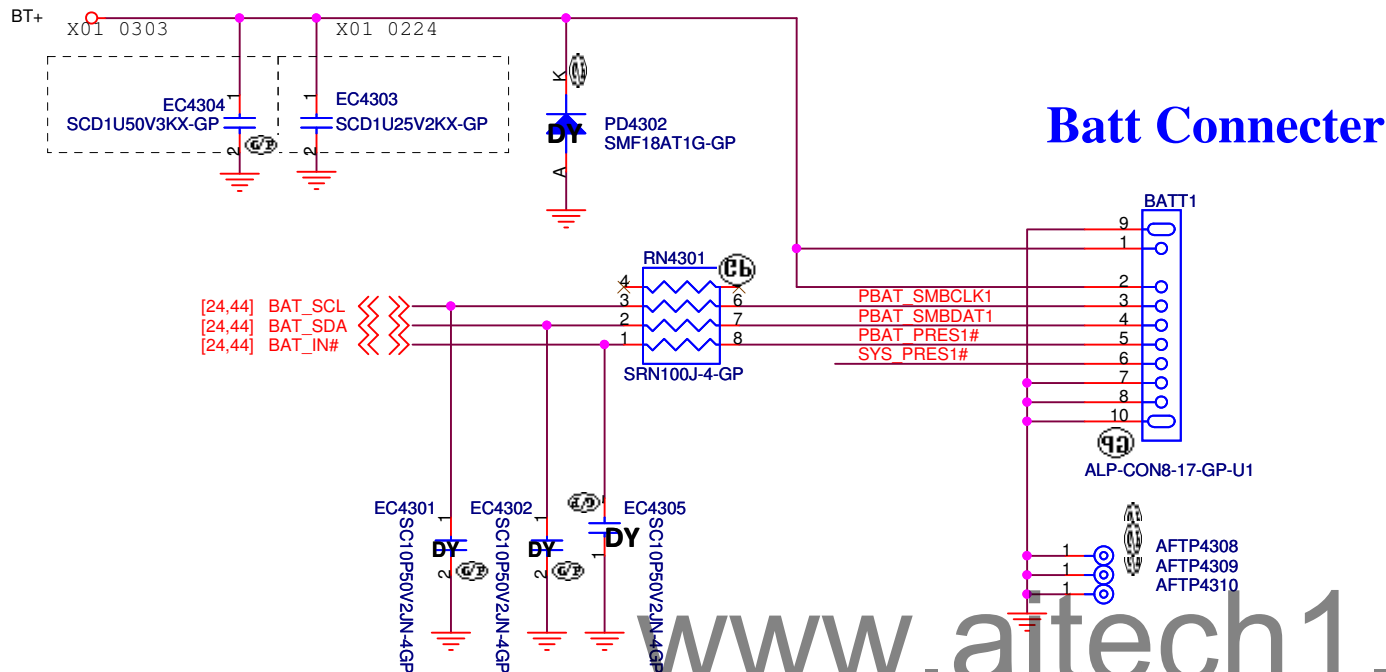
**Cottonwood**

Rev  
**A00**

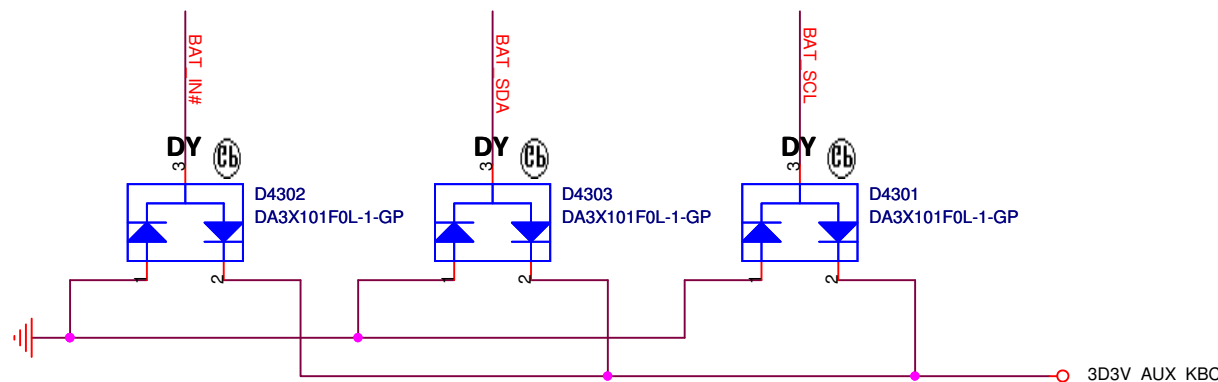
Date: Tuesday, June 17, 2014

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# SSID = PWR.Support



Placement: Close to Batt Connector



75.03101.07D

2nd = 83.00099.K11

3rd = 83.00099.M11

75.03101.07D

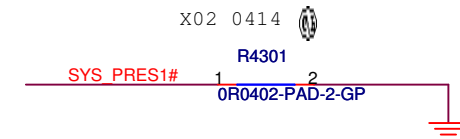
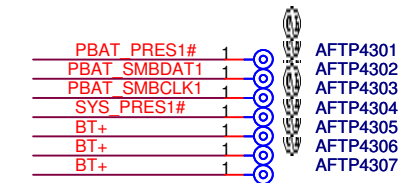
2nd = 83.00099.K11

3rd = 83.00099.M11

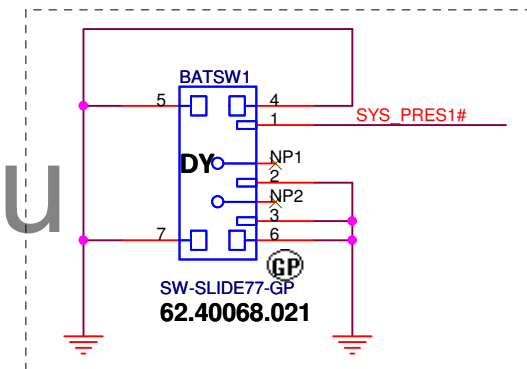
75.03101.07D

2nd = 83.00099.K11

3rd = 83.00099.M11



X01 0226



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Title

**BATT CONN**

Size  
A4

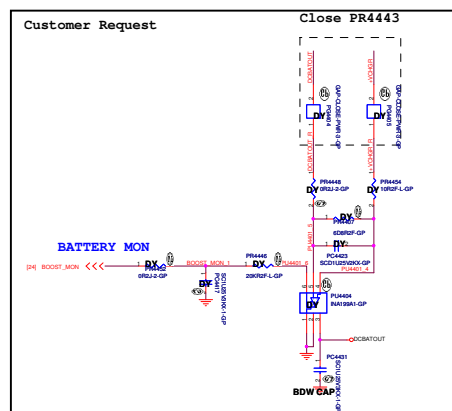
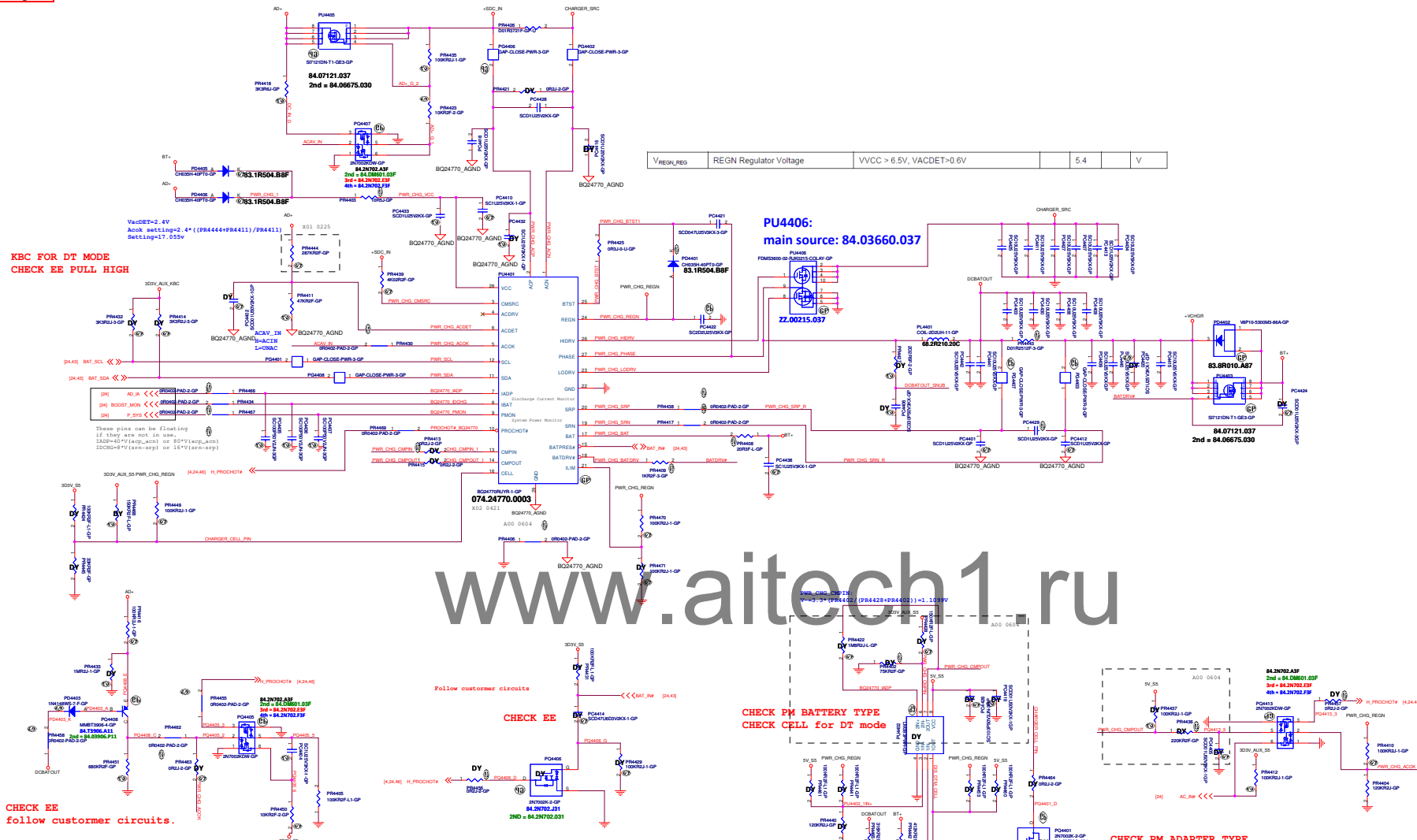
Document Number

**Cottonwood**

Rev  
A00

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ADAPTER TYPE	AD_IA_WW	AD_IA_WW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329
45W	L	H	0.659648



SSID = PWR.Plane.Regulator\_5v3p3v

Design Current=4A  
6A<OCP>6.5A

Design Current=6.7A  
10.6A<OCP>12.5A

Close to VFB Pin (pin5)

Close to VFB Pin (pin2)

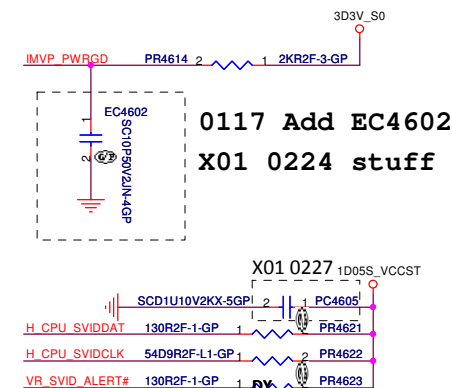
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKR 4.7UH PCMO63T-4R7MS Cyntec 28mohm/33mohm Isat =6.5Arms 68.4R71A.20H  
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L  
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	64.9K	13K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L  
Inductor: CHIP CHOKR 2.2U PCMO63T-2R2MM 18mohm/20mohm Isat =14Arms 68.2R210.20B  
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL /NEC/ 25mOhm / 77.C2271.45L  
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037  
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

```
SSID = CPU.Regulator
```

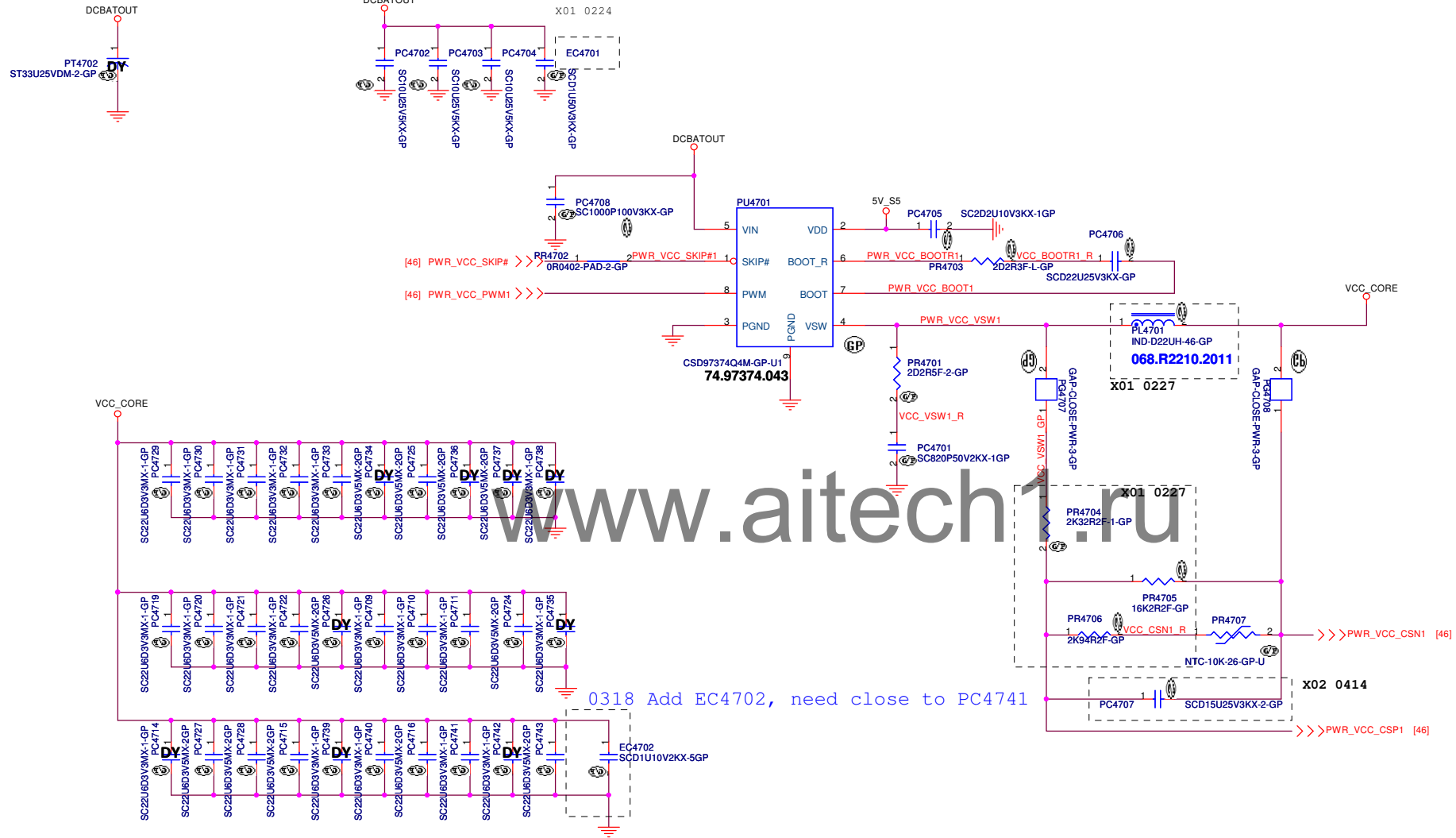


<Core Design>

	<p><b>Wistron Corporation</b>          21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,          Taipei Hsien 221, Taiwan, R.O.C.</p>
<p>Title</p>	
<p><b>046P TPS51624 CPUCORE(1/2)</b></p>	
<p>Size A3</p>	<p>Document Number</p>
<p><b>Cottonwood</b></p>	
<p>Date: Tuesday, June 17, 2014</p>	<p>Sheet 46 of 102</p>

SSID = CPU.Regulator

For acoustic noise



X01 0227  
(total:22uF/0603 x14pcs, 22uF/0805 x7pcs)

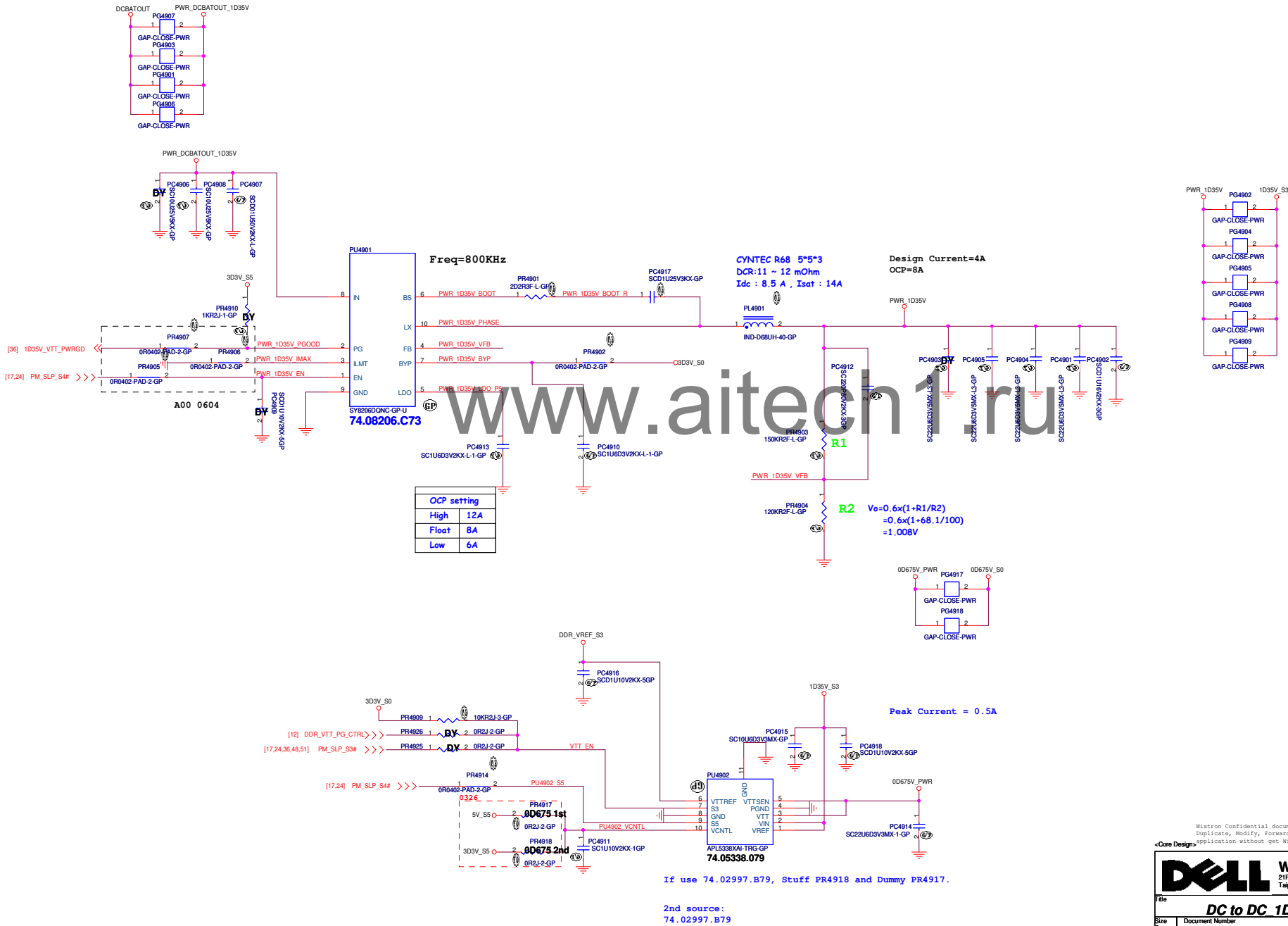
0318 Add EC4702, need close to PC4741

<Core Design>

## ***SY8208D for 1D05V***




## ***SY8206D for 1D35V***



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Title

Reserved

Size  
A3

Document Number  
Cottonwood

Date: Tuesday, June 17, 2014

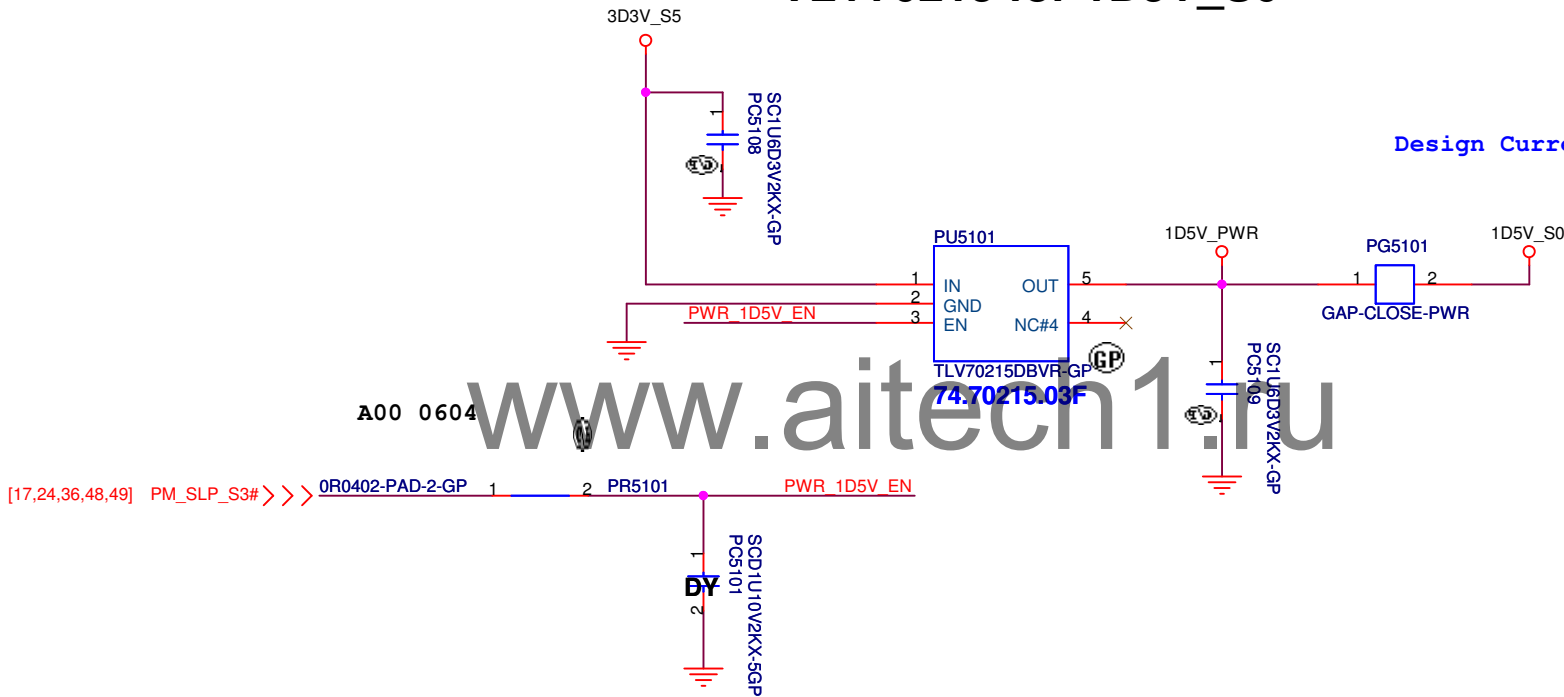
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SSID = PWR.Plane.Regulator\_1p5v

TLV70215 for 1D5V\_S0

Design Current = 150mA



<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
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Title			
<b>TPS51367 1D5V</b>			
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Date:	Tuesday, June 17, 2014	Sheet 51 of	104

## TOUCH PANEL POWER



(Blanking)

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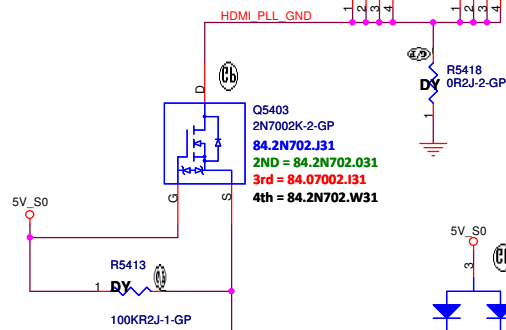
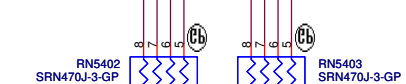
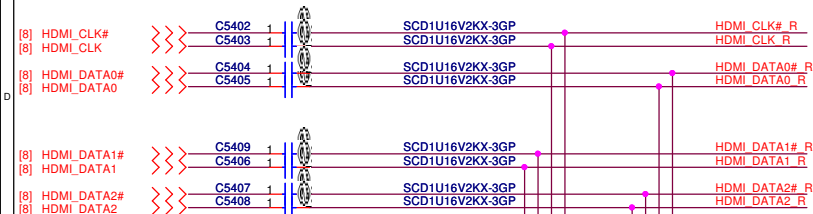
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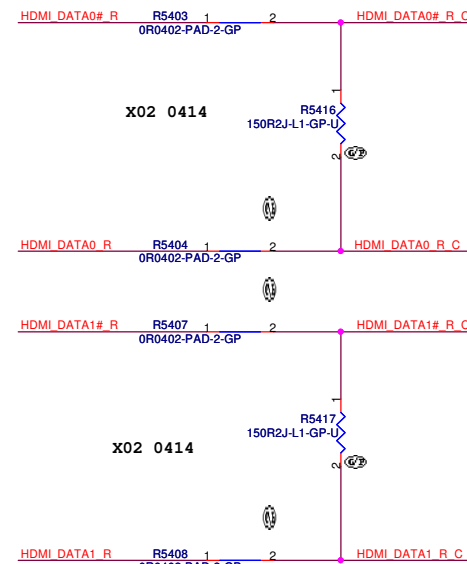
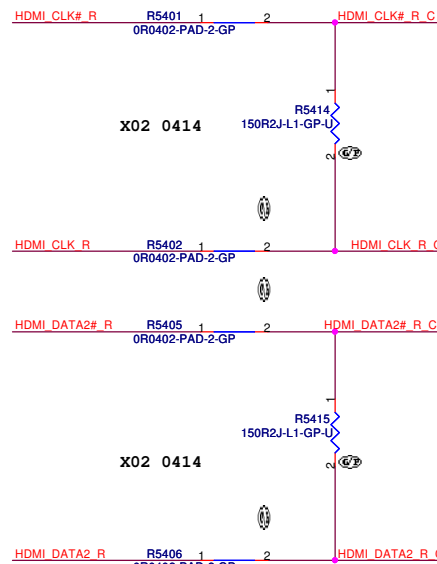
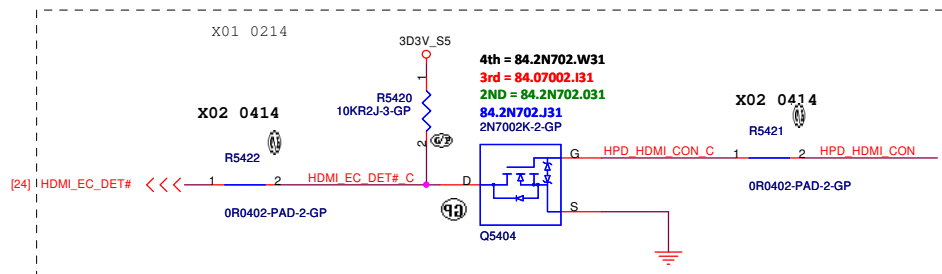
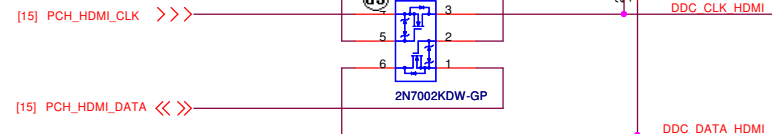
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Title			(Reserved)		
Size	Document Number				Rev
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Date: Tuesday, June 17, 2014			Sheet	53	of 104

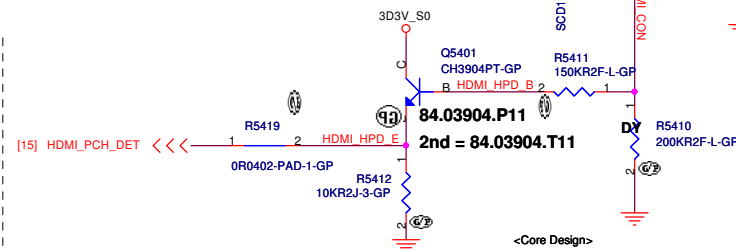
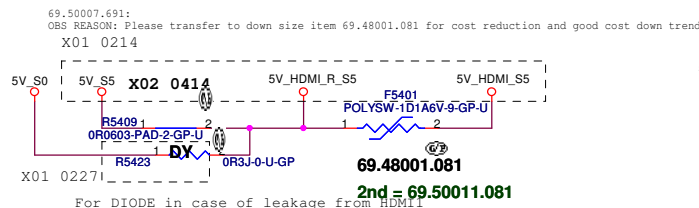
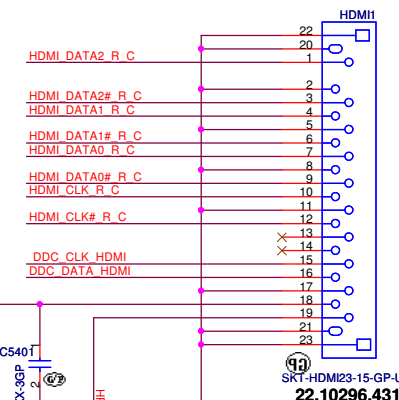
# SSID = VIDEO



84.2N702.A3F  
2nd = 84.2N702.E3F  
3rd = 75.00601.07C  
4th = 84.DMN66.03F



## HDMI CONN




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Title  
**(Reserved)DP to VGA Converter**

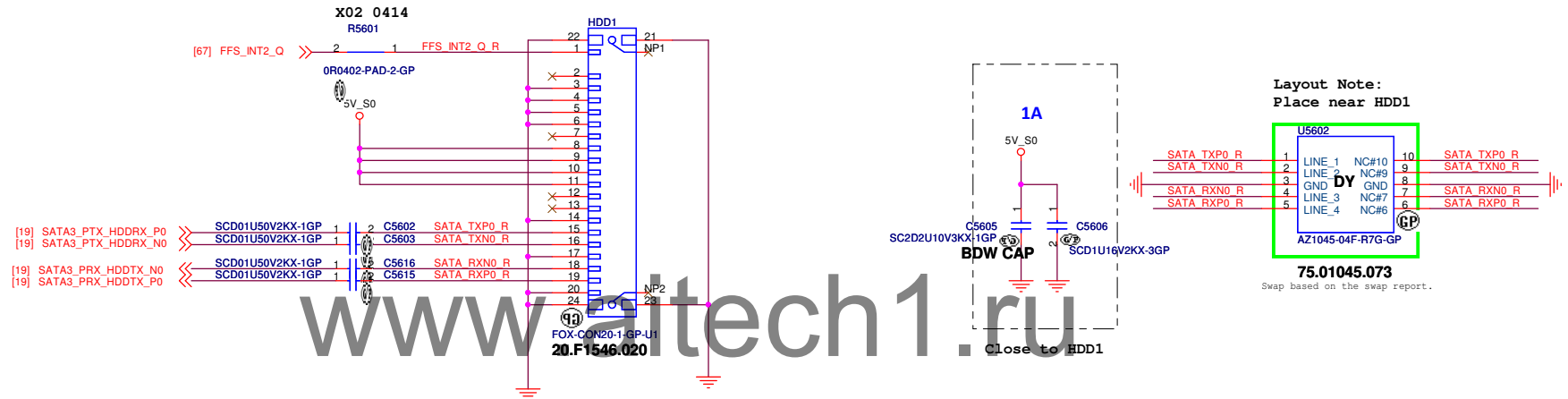
Size  
A3

Document Number  
**Cottonwood**

Rev  
**A00**

Date: Tuesday, June 17, 2014Sheet 55 of 104

## SATA HDD Connector




<Core Design>

SSID = ESATA

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(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

ESATA

Size

A3

Document Number

Cottonwood

Rev

A00

Date: Tuesday, June 17, 2014

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(Blanking)

www.altech1.ru

<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>WLAN (NGFF) CONN</b>		
Size	Document Number	Rev
A4	<b>Cottonwood</b>	<b>A00</b>
Date: Tuesday, June 17, 2014		Sheet 58 of 104

(Blanking)

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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(Blanking)

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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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SSID = User.Interface

(Blanking)

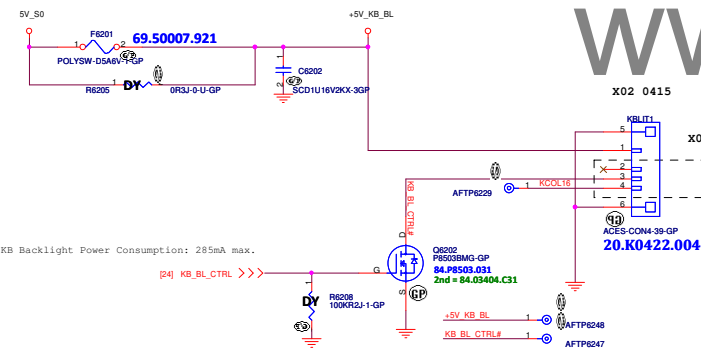
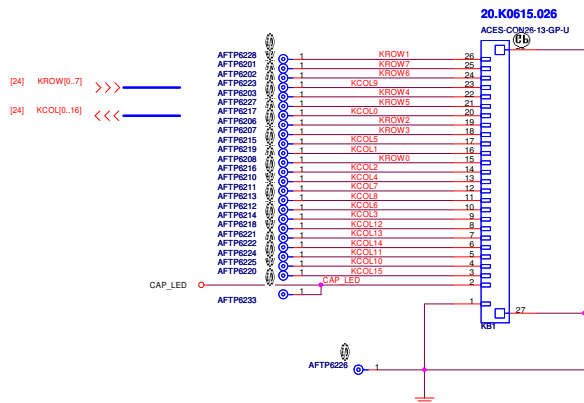
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LED Bard/Power Button</b>			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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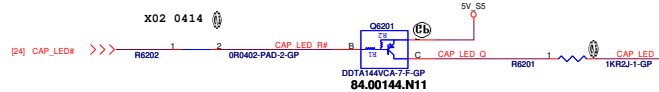
SSID = KBC

## Keyboard

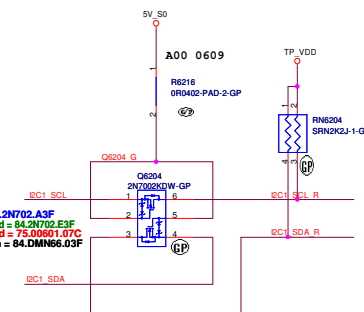
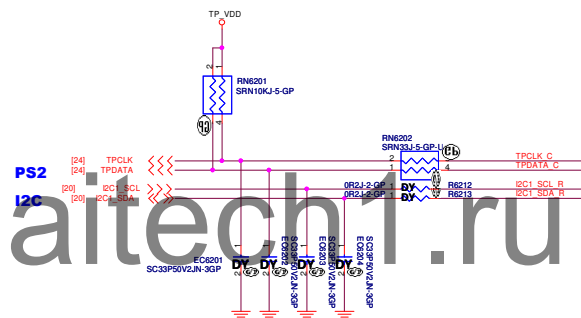
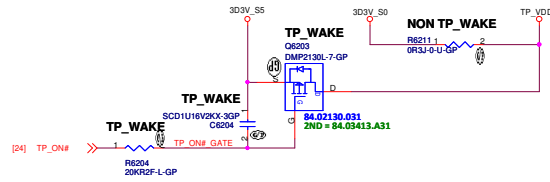


## CAP LED Control

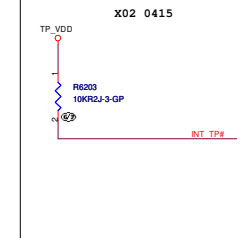
LOW active from KBC GPIO



## Touch.Pad

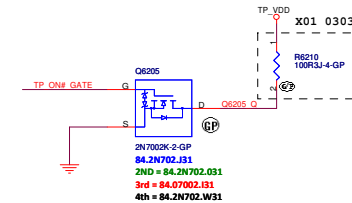


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.



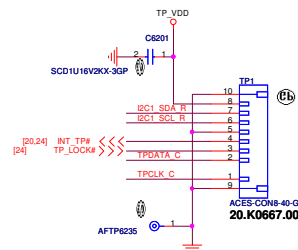
## X01 0214

TP\_VDD Discharge Circuit

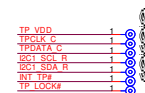


GPIO\_TPAD: TBD  
(Touch pad wake# for S3 wake up @ PCH GPIO??)

## Touch Pad Connector

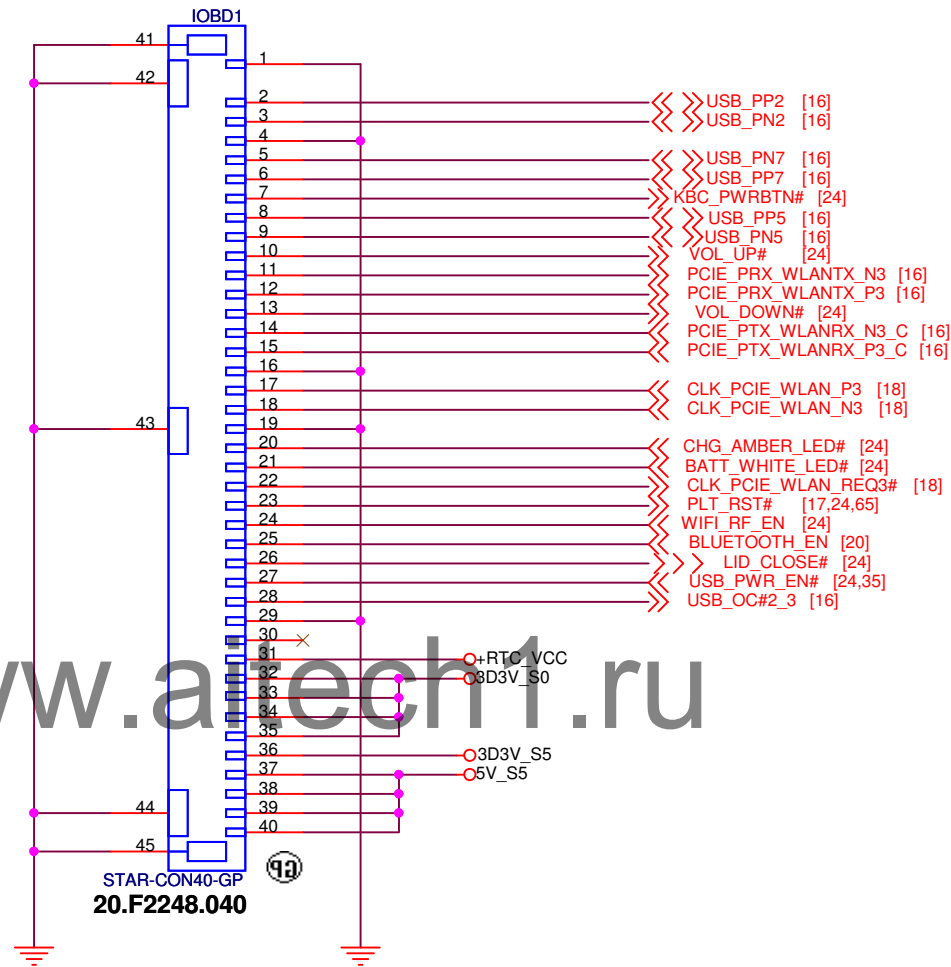


Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



«Core Design»

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Power Pin Count : 10  
GND Pin Count : 5

<Core Design>



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Title

**IO Board Connector**

Size  
A4

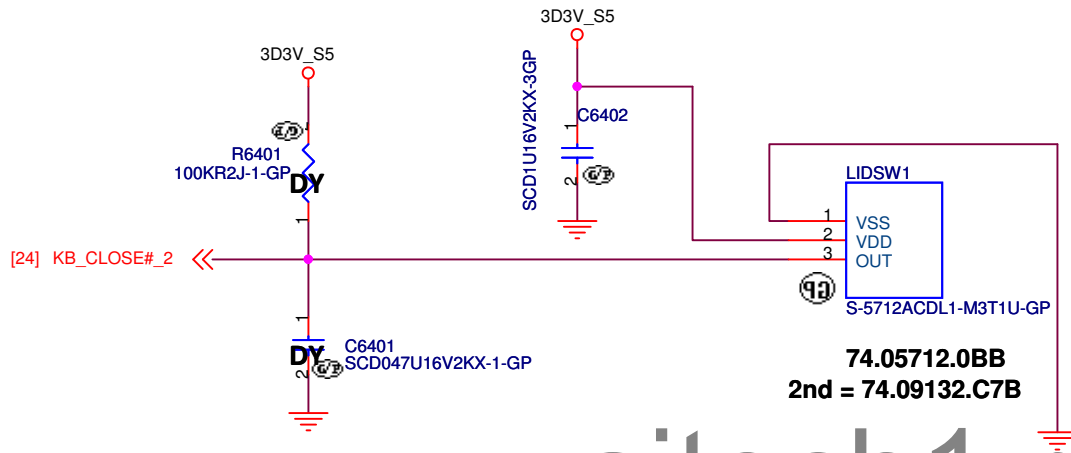
Document Number  
**Cottonwood**

Rev  
**A00**

Date: Tuesday, June 17, 2014


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SSID = User.Interface

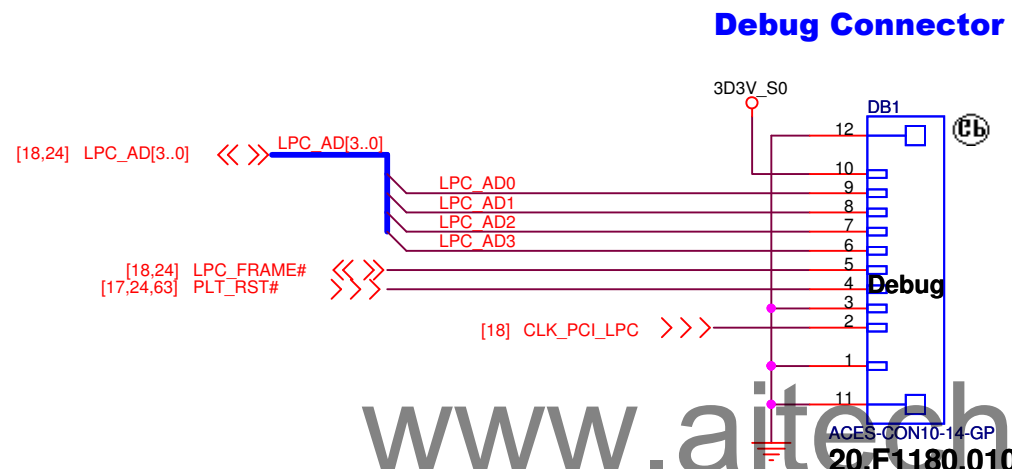


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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Hall Sensor</b>			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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SSID = DEBUG PORT



20.D0075.110: Dummy Pad with solder mask is ZZ.00PAD.Y41  
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

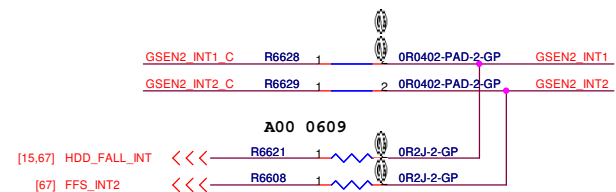
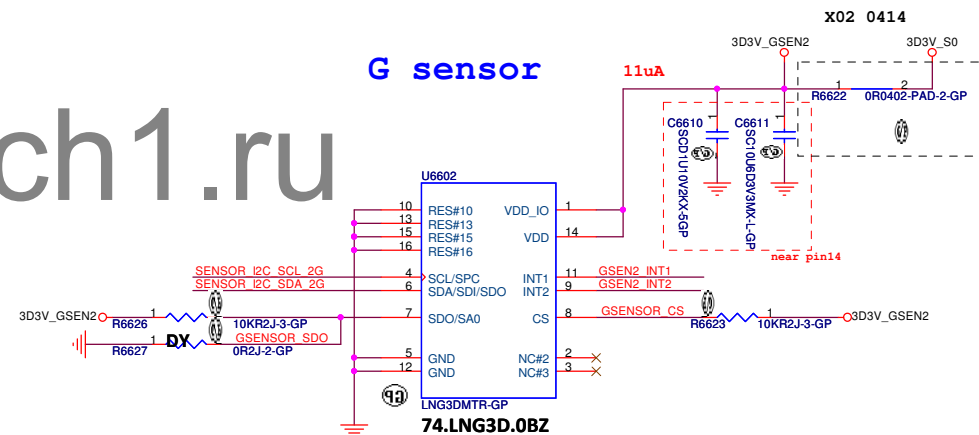
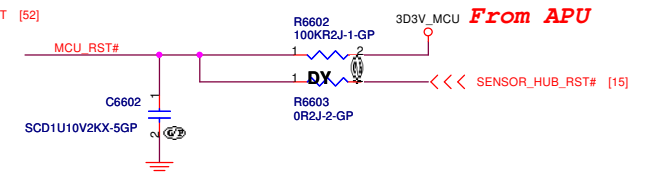
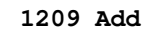
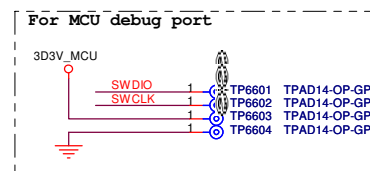
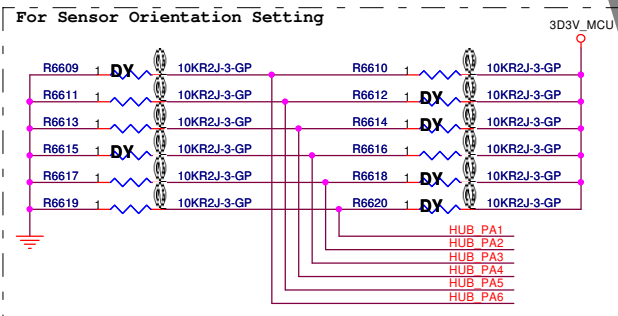
X01 0214



<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Dubug connector</b>			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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```
*Sensor HUB Version Differences
071.32151.000U is for Redwood
071.32151.0A0U is for Cottonwood
```



A00 0609

## <Core Design>

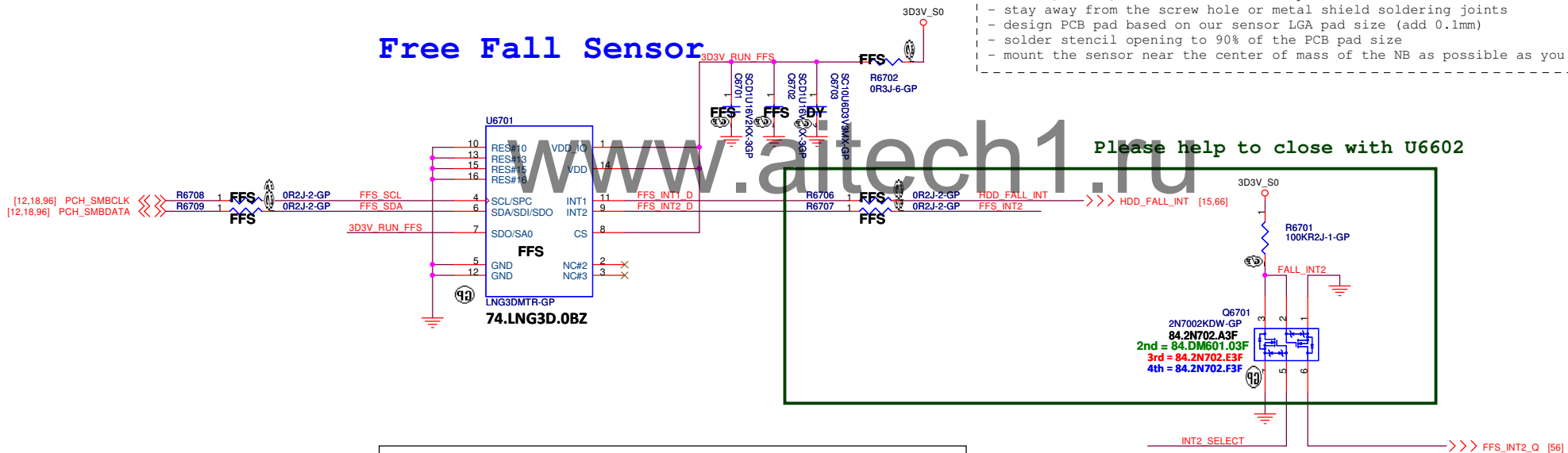


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Title	<b>Gyro / G sensor / E-compass</b>
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Size A3	Document Number <b>Cottonwood</b>	Rev <b>A00</b>
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## Free Fall Sensor



### Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

### Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602

<Core Design>



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Title

**Reserved**

Size  
A3

Document Number

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Rev

**A00**


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Title

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Title

**USB3.0 PORT**

Size  
A3

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**A00**

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Title

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Size  
A3

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Title

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A3	<i>Cottonwood</i>	<b>A00</b>

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Title

Reserved

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Rev  
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<Core Design>			
<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsien Tai Wu Rd., Hsuehshen, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU_PCIE/STRAPPING(1/5)</b>			
Size	Document Number		Rev
A2	<b>Cottonwood</b>		<b>A00</b>
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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>GPU_DPPWR/GND(5/5)</b>			
Size Custom	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
Date Tuesday, June 17, 2014	Sheet 77	of 104	

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Title			
<b>GPU-VRAM1,2 (1/4)</b>			
Size A3	Document Number		Rev
	<b>Cottonwood</b>		<b>A00</b>
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>GPU-VRAM3,4 (2/4)</b>			
Size A3	Document Number		Rev
	<b>Cottonwood</b>		<b>A00</b>
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### <Core Design>



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	Title
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**GPU-VRAM5,6 (3/4)**

Size	A3
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Document Number	
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## Cottonwood

Rev

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**A00**

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<Core Design>			
		<b>Wistron Corporation</b> 21F, 6th, Sec. 1, Hsin Te Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>RT8812 VGACORE</b>			
Size A2	Document Number <b>Cottonwood</b>	Rev <b>A00</b>	
Date: Tuesday, June 17, 2014		Sheet 82 of	104

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<Core Design>			
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Neichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		<b>DISCRETE VGA POWER</b>	
Size	Document Number	Rev	
Custom	<b>Cottonwood</b>	<b>A00</b>	
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Title

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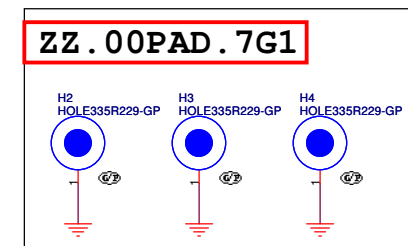
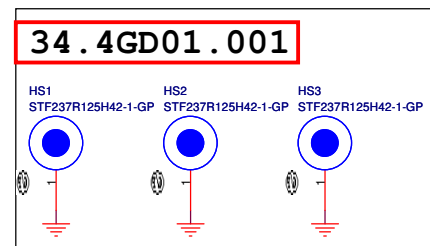
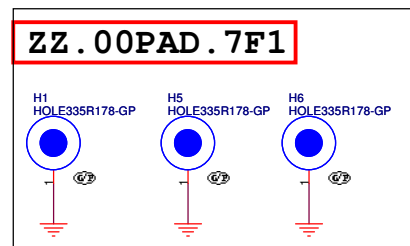
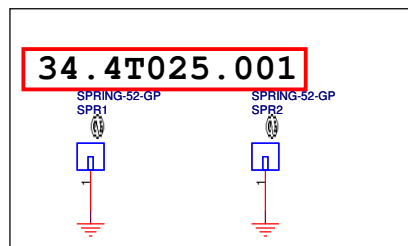
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**Reserved**

Size	Document Number	Rev
A3	<b>Cottonwood</b>	<b>A00</b>

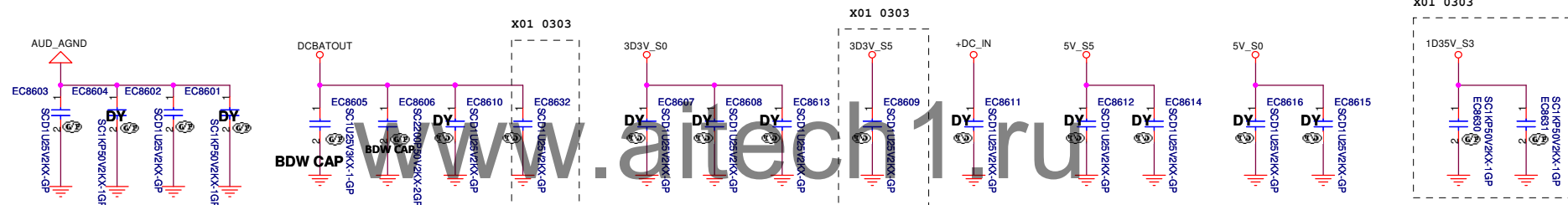
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## SSID = Mechanical

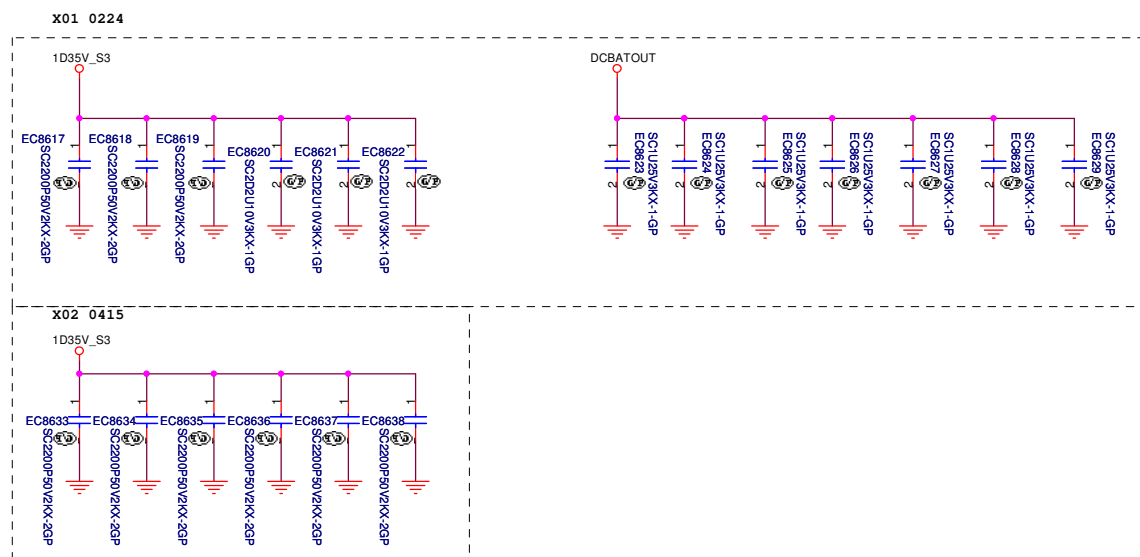


## SSID = EMI

Mind the voltage rating of the caps.



## SSID = RF



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**DELL** Wistron Corporation  
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Title	UNUSED PARTS/EMI Capacitors		
Size	Document Number	Rev	A00
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Size  
A3

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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>(Reserved)Finger Print</b>			
Size A4	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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Title

**Free Fall Sensor**

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Title

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Size  
A3

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<Core Design>



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Title

**Reserved**


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<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Express Card</b>			
Size A3	Document Number <b>Cottonwood</b>		Rev <b>A00</b>
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Title

**LVDS Switch**

Size A3	Document Number <b>Cottonwood</b>	Rev <b>A00</b>
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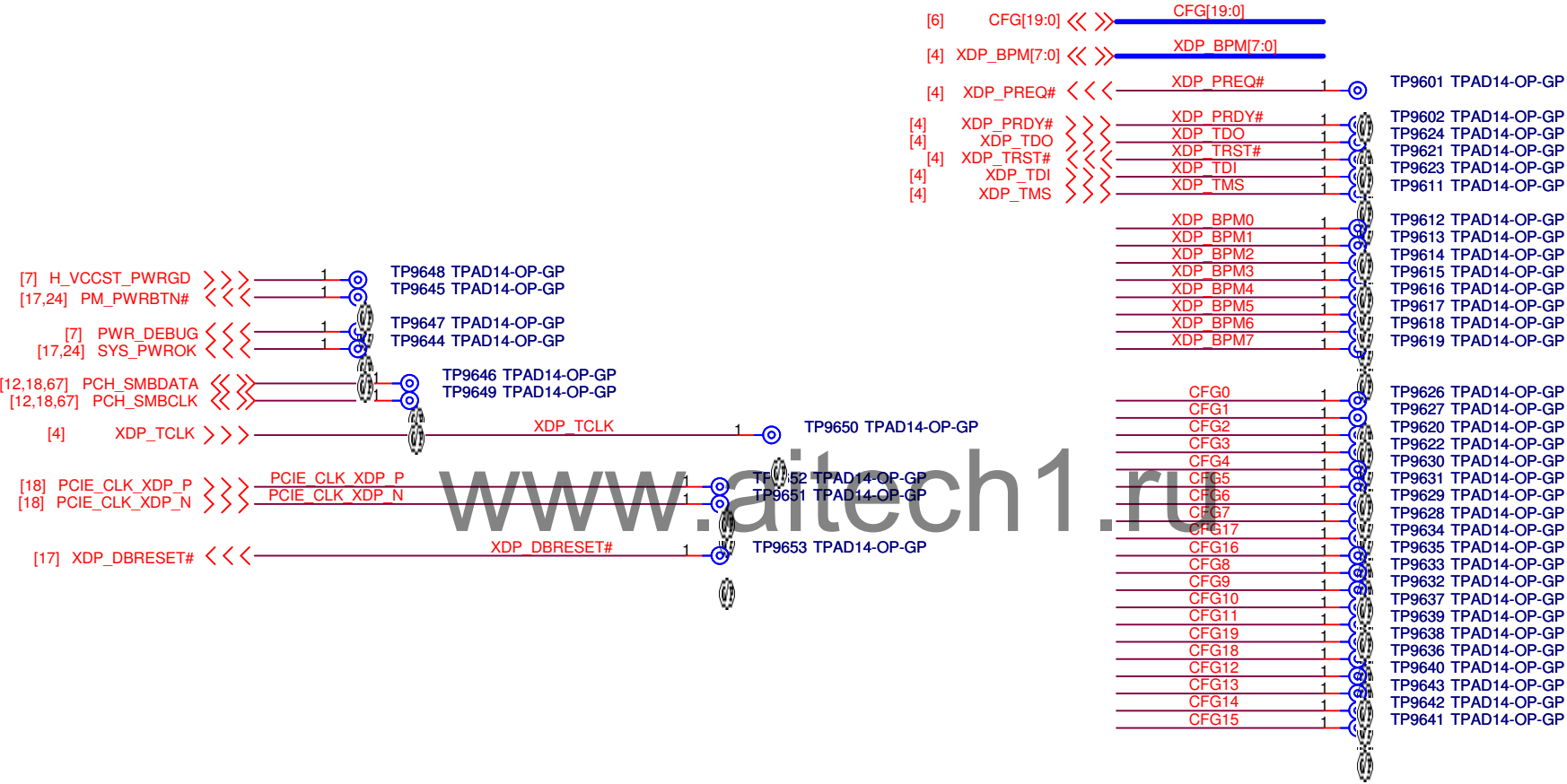
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CRT Switch</b>			
Size A3	Document Number	Rev	
<b>Cottonwood</b>		<b>A00</b>	
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SSID = XDP

CPU XDP



<Core Design>



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Title

**CPU/PCH XDP**

Size  
A4

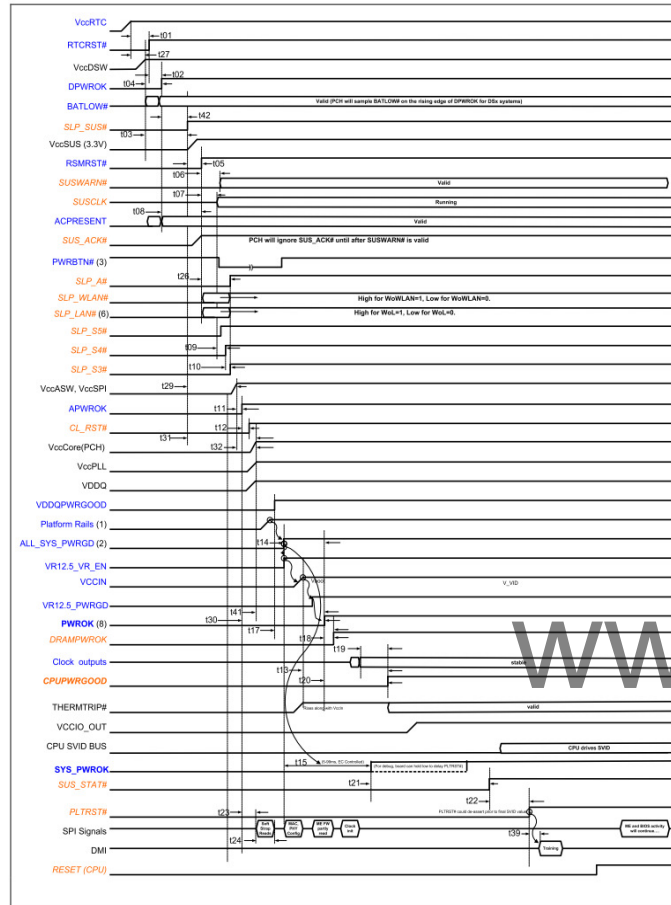
Document Number  
**Cottonwood**

Rev  
**A00**

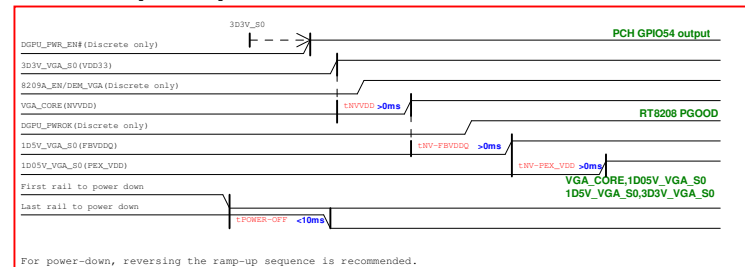
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## Shark Bay Platform Power Sequence

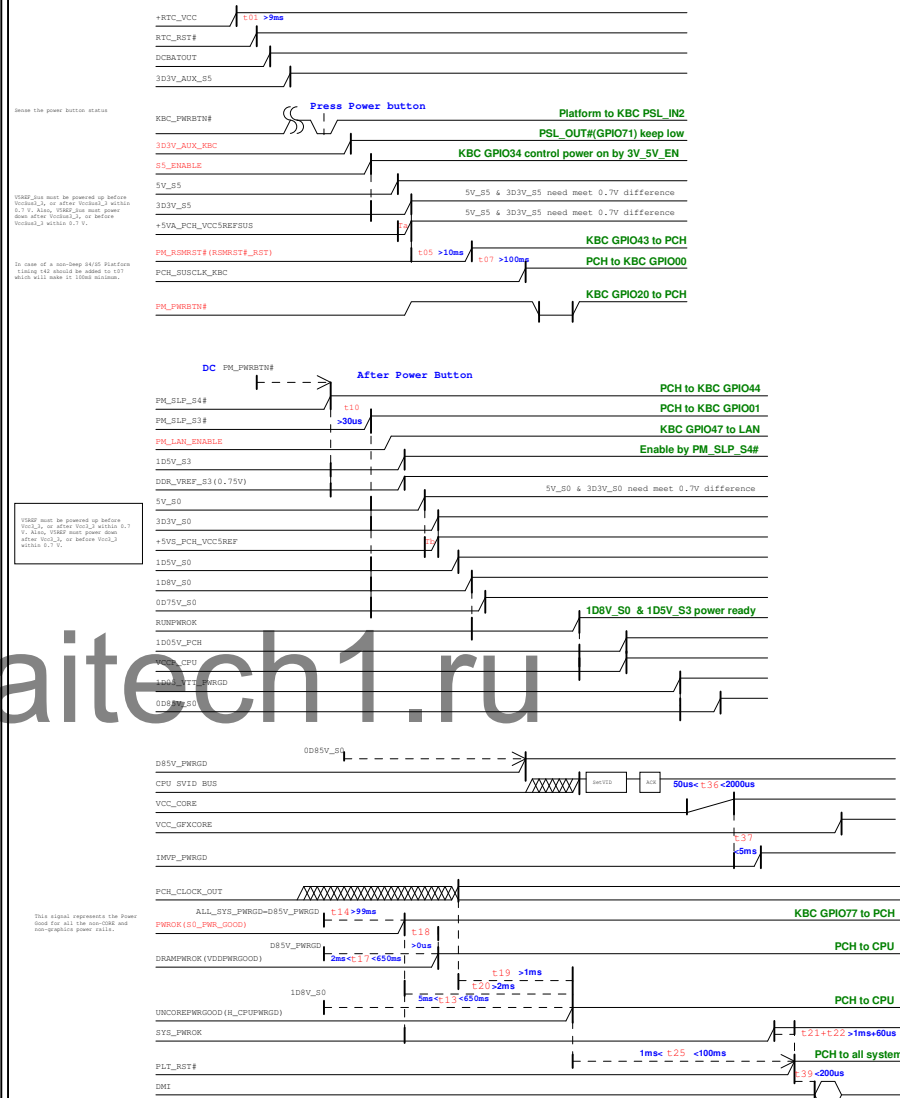


### N14P-GT Power-Up/Down Sequence

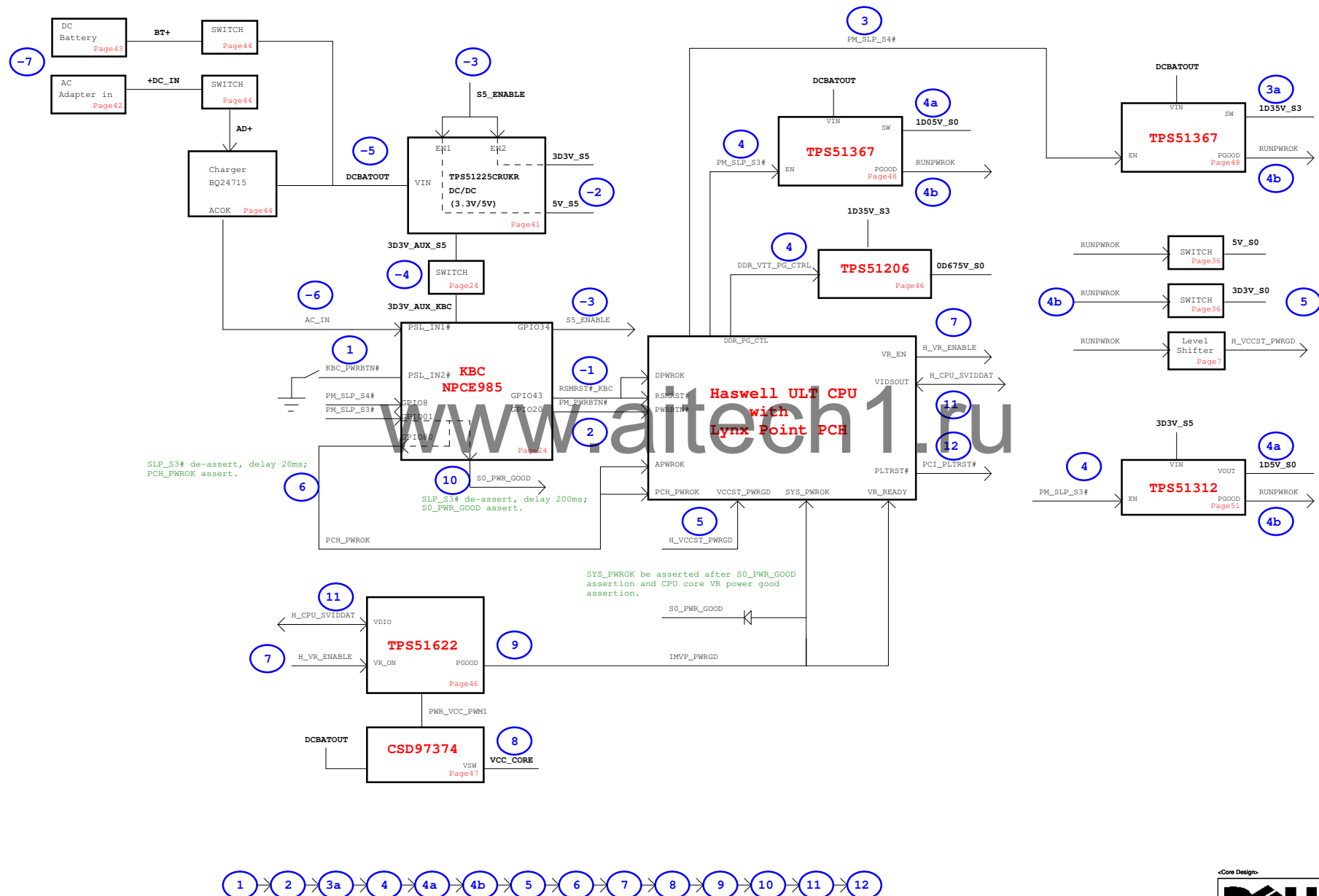


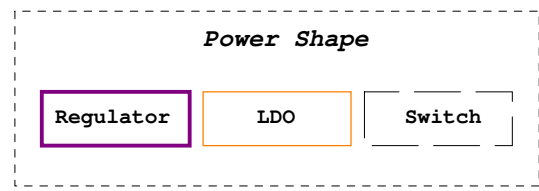
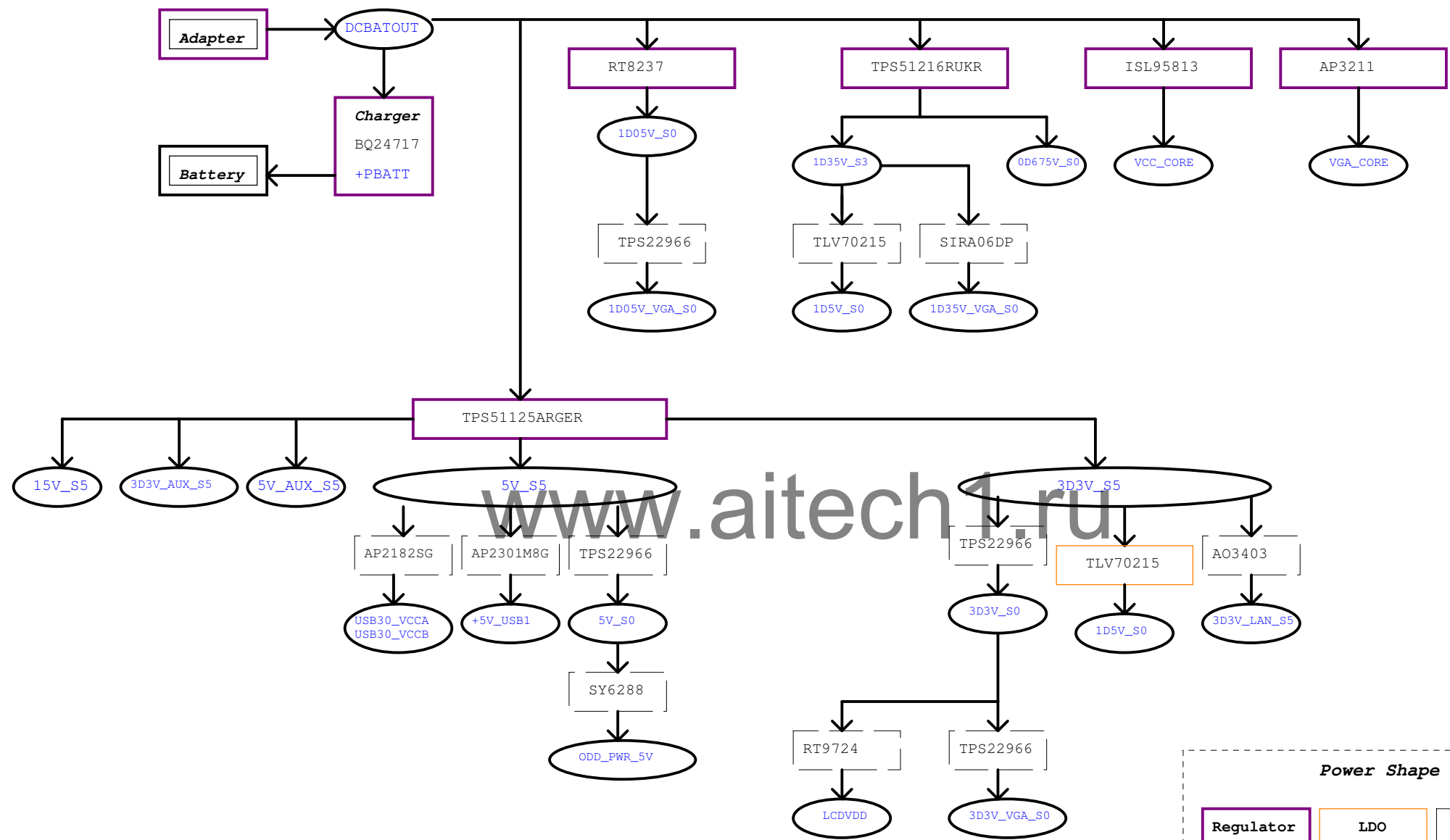
(DC mode)

Red Words: Controlled by EC GPIC



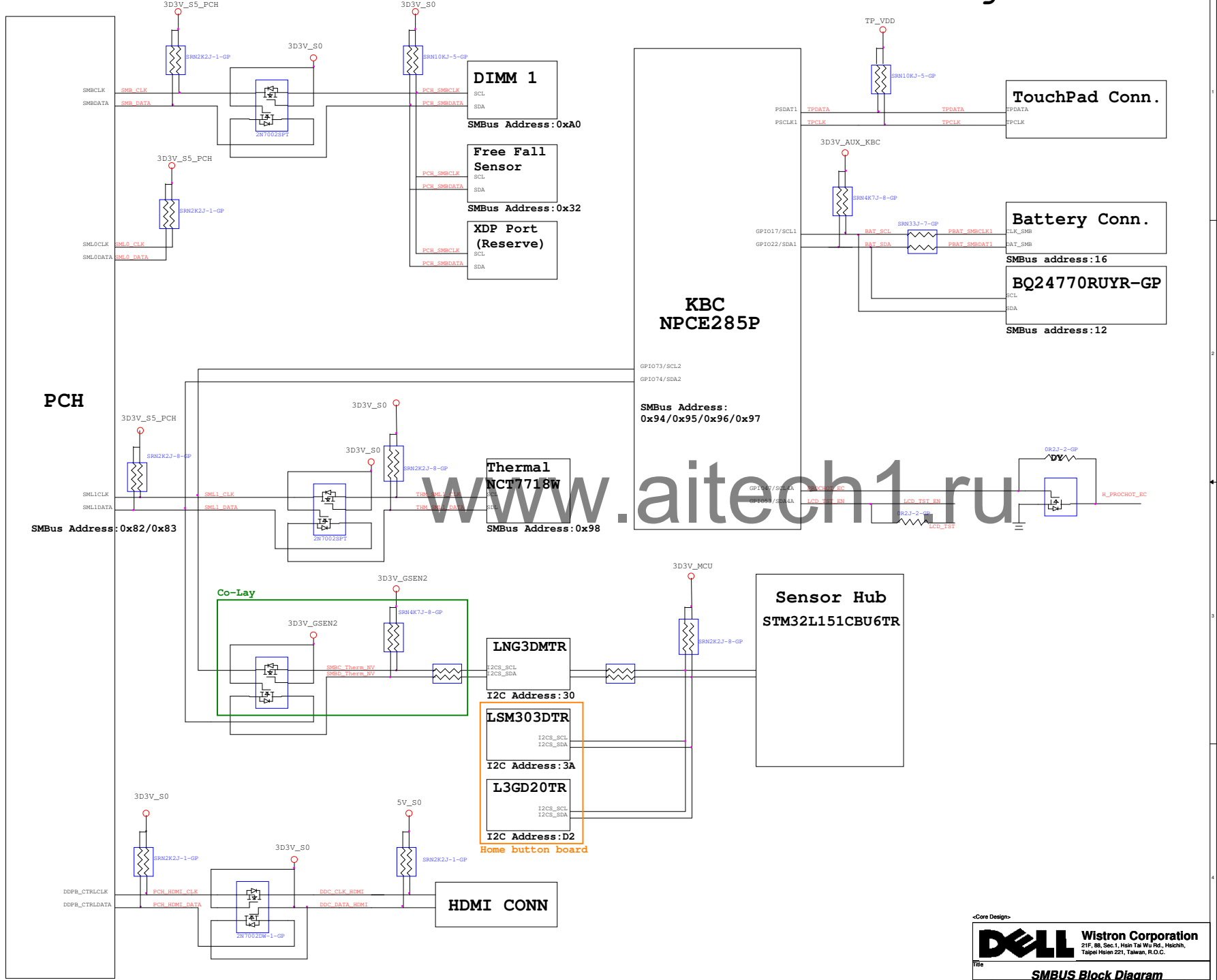
# Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM





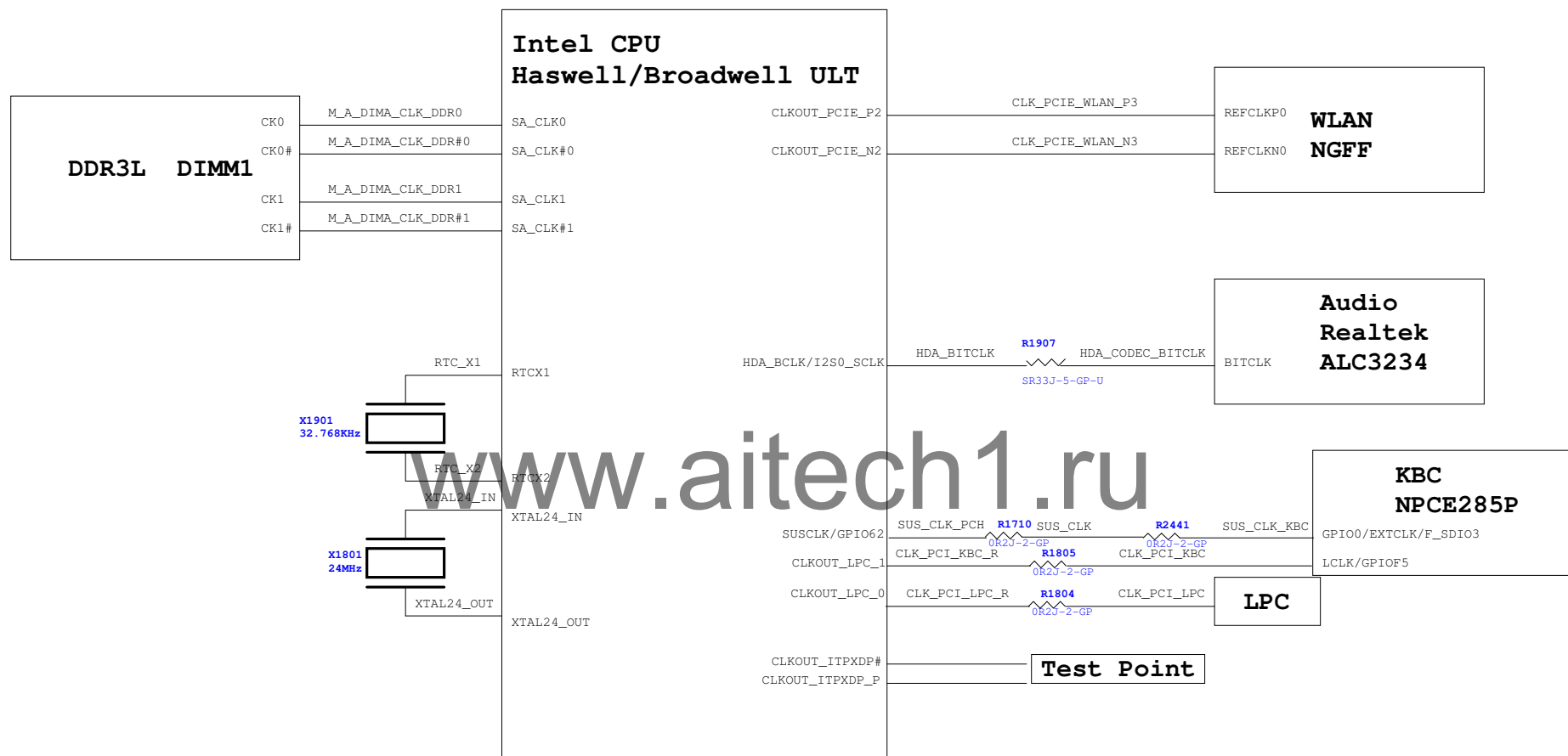
PCH SMBus Block Diagram

KBC SMBus Block Diagram

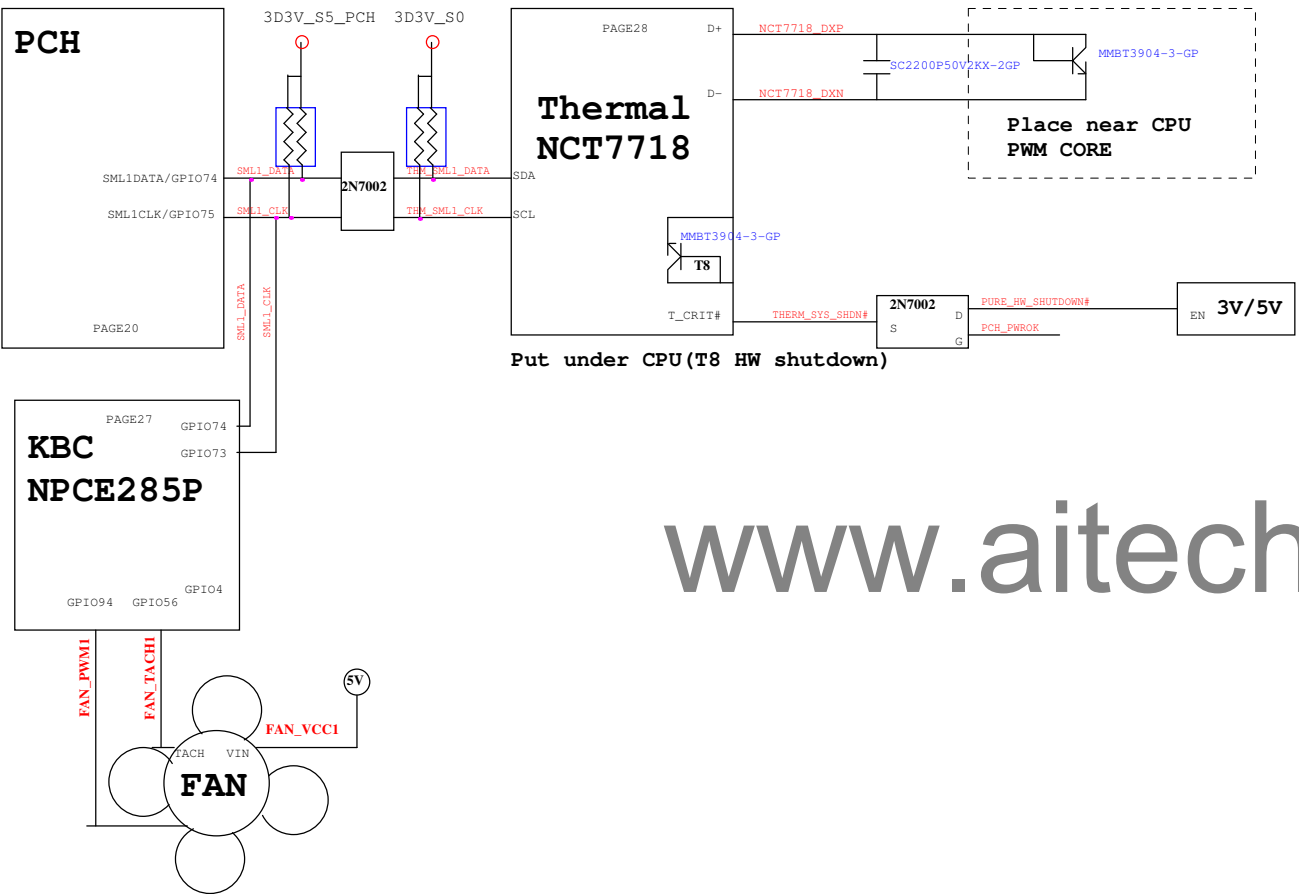




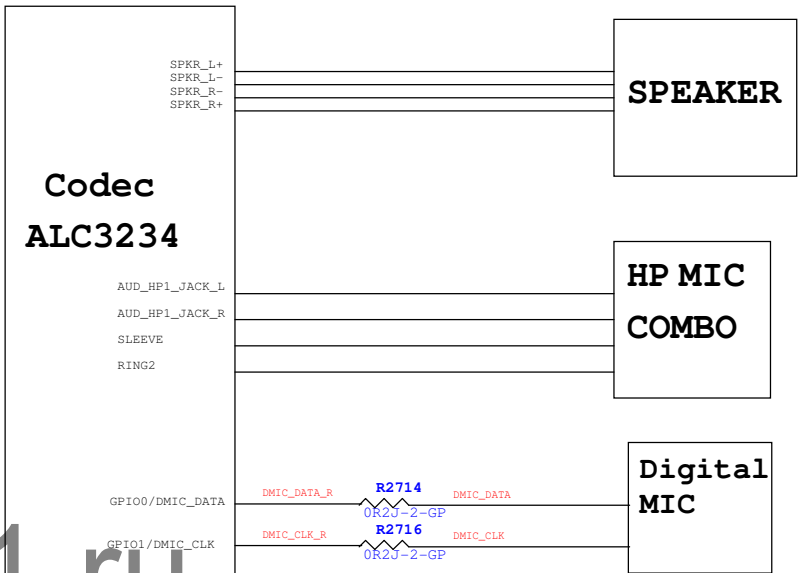
# CLK Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



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